METHOD AND APPARATUS FOR REDUCING DC OFFSETS IN A COMMUNICATION SYSTEM

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The following applications of common assignee are related to the present application, and are herein incorporated by reference in their entireties:

STATEMENT REGARDING FEDERALLY-SPONSORED RESEARCH AND DEVELOPMENT

[0002] Not applicable.

REFERENCE TO MICROFICHE APPENDIX/SEQUENCE LISTING/TABLE/COMPUTER PROGRAM LISTING APPENDIX (submitted on a compact disc and an incorporation-by-reference of the material on the compact disc)

[0003] Not applicable.

BACKGROUND OF THE INVENTION

Field of the Invention

[0004] The present invention relates to frequency conversion of electromagnetic (EM) signals. More particularly, the present invention relates to reducing or eliminating DC offset voltages when down-converting a signal in a communication system.

Background Art

[0005] Electromagnetic (EM) information signals (baseband signals) include, but are not limited to, video baseband signals, voice baseband signals, computer baseband signals, etc. Baseband signals include analog baseband signals and digital baseband signals. It is often beneficial to propagate baseband signals at higher frequencies. Conventional up-conversion processes use modulation techniques to modulate higher frequency carrier signals with the baseband signals, to form modulated carrier signals.

[0006] Numerous problems exist in attempting to accurately receive or down-convert modulated carrier signals in communication systems. One such problem is when unwanted DC offset voltages exist in receiver channels. A DC offset voltage may enter a receiver channel by way of receiver channel down-conversion circuitry components, for example. This unwanted DC offset can enter a receiver channel, and cause the receiver channel to become saturated. For example, DC offset may saturate a receiver channel when it is amplified by gain amplifiers in the receiver channel, such that a voltage rail is reached or exceeded. Furthermore, any DC offset in the receiver channel has the effect of competing with the signal of interest, producing a statistical bias much like an interference. Hence, it is desirable to reduce or entirely

eliminate unwanted DC offset voltages from receiver channels. Furthermore, the DC offset voltages must be removed without distorting the signal of interest.

BRIEF SUMMARY OF THE INVENTION

[0007] Methods and apparatuses for reducing DC offsets in a communication system are described. In a first embodiment, a first receiver channel signal is received from a first receiver channel node. The first receiver channel signal is integrated to generate an integrated signal. The integrated signal is summed with a second receiver channel signal at a second receiver channel node. The first receiver channel node is downstream from the second receiver channel node in the receiver channel.

[0008] In an embodiment, a feedback loop circuit is used to reduce DC offsets in the WLAN receiver channel, according to the above stated method. A receiver channel signal is coupled as a first input to a summing node in the receiver channel. An integrator has an input coupled to a second node of the receiver channel. An output of the integrator is coupled as a second input to the summing node.

[0009] The frequency response of the feedback loop circuit may be variable. In such an embodiment, the integrator has a frequency response that may be controlled to vary the frequency response of the feedback loop circuit. By varying the frequency response of the feedback loop circuit, the frequency response of the receiver channel may be varied. For example, the integrator frequency response may be varied to vary the frequency response of the receiver channel to a first frequency response, a second frequency response, and a third frequency response. Each of the three frequency responses have a corresponding lower 3 dB frequency. The first frequency response may have a relatively low lower 3 dB frequency. The second frequency response may have a relatively medium lower 3 dB frequency. The third frequency response may have a relatively greater lower 3 dB frequency.

[0010] In a second embodiment, a circuit provides gain control in a communication system, such as a WLAN receiver channel. A first automatic gain control (AGC) amplifier is coupled in a first portion of the receiver channel. A second AGC amplifier is coupled in a second portion of the receiver channel. The second AGC amplifier receives a first AGC signal. The first AGC amplifier receives a second AGC signal. The first and second AGC signals are related to each other. In an example embodiment, a multiplier receives the first AGC signal and outputs the second AGC signal.

[0011] Methods and apparatuses for monitoring DC offset, and for providing control signals for varying the frequency response of the DC offset reducing circuits are provided. In an embodiment, a window comparator module determines whether a DC offset in each of an I channel input signal and a Q channel input signal is within an acceptable range. In an embodiment, a state machine generates the control signals that vary circuit frequency responses.

[0012] Further embodiments, features, and advantages of the present inventions, as well as the structure and operation of the various embodiments of the present invention, are described in detail below with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0013] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

[0014] FIG. 1A is a block diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

[0015] FIG. 1B is a more detailed diagram of a universal frequency translation (UFT) module according to an embodiment of the invention.

[0016] FIG. 1C illustrates a UFT module used in a universal frequency down-conversion (UFD) module according to an embodiment of the invention.

[0017] FIG. 1D illustrates a UFT module used in a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0018] FIG. 2 is a block diagram of a universal frequency translation (UFT) module according to an alternative embodiment of the invention.

[0019] FIGs. 3A and 3G are example aliasing modules according to embodiments of the invention.

[0020] FIGs. 3B-3F are example waveforms used to describe the operation of the aliasing modules of FIGs. 3A and 3G.

[0021] FIG. 4 illustrates an energy transfer system with an optional energy transfer signal module according to an embodiment of the invention.

[0022] FIG. 5 illustrates an example aperture generator.

[0023] FIG. 6A illustrates an example aperture generator.

[0024] FIG. 6B illustrates an oscillator according to an embodiment of the present invention.

[0025] FIGs. 7A-B illustrate example aperture generators.

[0026] FIG. 8 illustrates an aliasing module with input and output impedance match according to an embodiment of the invention.

[0027] FIG. 9 illustrates an example energy transfer module with a switch module and a reactive storage module according to an embodiment of the invention.

[0028] FIG. 10 is a block diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0029] FIG. 11 is a more detailed diagram of a universal frequency up-conversion (UFU) module according to an embodiment of the invention.

[0030] FIG. 12 is a block diagram of a universal frequency up-conversion (UFU) module according to an alternative embodiment of the invention.

[0031] FIGs. 13A-13I illustrate example waveforms used to describe the operation of the UFU module.

[0032] FIG. 14 illustrates a unified down-converting and filtering (UDF) module according to an embodiment of the invention.

[0033] FIG. 15 illustrates an exemplary I/Q modulation embodiment of a receiver according to the invention.

[0034] FIG. 16 shows an exemplary receiver channel in which embodiments of the present invention may be implemented.

[0035] FIG. 17 shows an receiver channel with automatic gain control, according to an embodiment of the present invention.

[0036] FIG. 18 shows a DC offset voltage present in an example model of an operational amplifier gain stage.

[0037] FIG. 19 shows an example feedback loop for reducing DC offset in a receiver channel, according to an embodiment of the present invention.

[0038] FIG. 20 shows an exemplary differentiator circuit that may be used to reduce or eliminate DC offset voltages in the receiver channel.

[0039] FIG. 21 shows an example embodiment for the integrator of FIG. 19, including an operational amplifier, a resistor, and a capacitor that are configured in an integrating amplifier configuration.

[0040] FIG. 22 shows an embodiment of the feedback loop of FIG. 19, where the first amplifier is divided into a first feedback amplifier and a second feedback amplifier, according to the present invention.

[0041] FIG. 23 shows an integrator, where the resistor is a variable resistor, according to an embodiment of the present invention.

[0042] FIG. 24A shows a frequency response of an ideal integrator similar to the integrator of FIG. 19.

[0043] FIG. 24B shows a plot of the frequency response of the feedback loop of FIG. 19.

[0044] FIG. 25A shows frequency responses for the integrator of FIG. 19 during three time periods, according to an embodiment of the present invention.

[0045] FIG. 25B shows frequency responses for the feedback loop of FIG. 19 that correspond to first, second, and third frequency responses shown in FIG. 25A.

[0046] FIG. 26 shows an example embodiment for the multiplier shown in FIG. 17.

[0047] FIGS. 27-29 and 33-34 show example flowcharts providing operational steps for performing embodiments of the present invention.

[0048] FIG. 30 shows a differential UFD module that may be used as a down-converter, according to an embodiment of the present invention.

[0049] FIGS. 31A and 31B show further detail of a receiver channel, according to an exemplary embodiment of the present invention.

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[0050] FIGS. 32A and 32B show further detail of a receiver channel, according to an example differential receiver channel embodiment of the present invention.

[0051] FIGS. 35-37 show exemplary frequency responses for a receiver channel configured as shown in FIGS. 31A-B or 32A-B, when the frequency response is varied, according to embodiments of the present invention.

[0052] FIG. 38 shows example waveforms related to the operation of receiver channel as shown in FIGS. 32A-B in a WLAN environment, according to an embodiment of the present invention.

[0053] FIG. 39 shows an example timeline for receiving a WLAN DSSS frame, according to an embodiment of the present invention.

[0054] FIG. 40 shows an example 1/f noise characteristic curve.

[0055] FIG. 41 shows a high level view of a window comparator module, according to an embodiment of the present invention.

[0056] FIGS. 42 and 43 show more detailed examples of the window comparator module of FIG. 41, according to embodiments of the present invention.

[0057] FIG. 44 shows example waveforms related to the operation of a waveform comparator, according to an embodiment of the present invention.

[0058] FIG. 45 shows an example state machine module for generating and sequencing control signals of the present invention.

[0059] FIGS. 46 and 47 show example state diagrams that may be implemented by the state machine module of FIG. 45, according to embodiments of the present invention.

[0060] FIGS. 48-50 and 52 show example flowcharts providing operational steps for performing embodiments of the present invention.

[0061] FIG. 51 shows an block diagram of an integrator that receives a control signal, according to an embodiment of the present invention.

[0062] The present invention will now be described with reference to the accompanying drawings. In the drawings, like reference numbers generally indicate identical or functionally similar elements. Additionally, the left-most digit(s) of a reference number generally identifies the drawing in which the reference number first appears.

DETAILED DESCRIPTION OF THE INVENTION

Table of Contents

1. Introduction

[0063] The present invention is directed to the down-conversion and up-conversion of an electromagnetic signal using a universal frequency translation (UFT) module, transforms for same, and applications thereof. The systems described herein each may include one or more receivers, transmitters, and/or transceivers. According to embodiments of the invention, at least some of these receivers, transmitters, and/or transceivers are implemented using universal frequency translation (UFT) modules. The UFT modules perform frequency translation operations. Embodiments of the present invention are described below.

[0064] Systems that transmit and receive EM signals using UFT modules exhibit multiple advantages. These advantages include, but are not limited to, lower power consumption, longer power source life, fewer parts, lower cost, less tuning, and more effective signal transmission and reception. These systems can receive and transmit signals across a broad frequency range. The structure and operation of embodiments of the UFT module, and various applications of the same are described in detail in the following sections, and in the referenced documents.

2. Universal Frequency Translation

[0065] The present invention is related to frequency translation, and applications of same. Such applications include, but are not limited to, frequency down-conversion, frequency up-conversion, enhanced signal reception, unified down-conversion and filtering, and combinations and applications of same.

[0066] FIG. 1A illustrates a universal frequency translation (UFT) module 102 according to embodiments of the invention. (The UFT module is also sometimes called a universal frequency translator, or a universal translator.)

[0067] As indicated by the example of FIG. 1A, some embodiments of the UFT module 102 include three ports (nodes), designated in FIG. 1A as Port 1, Port 2, and Port 3. Other UFT embodiments include other than three ports.

[0068] Generally, the UFT module 102 (perhaps in combination with other components) operates to generate an output signal from an input signal, where the frequency of the output signal differs from the frequency of the input signal. In other words, the UFT module 102 (and perhaps other components) operates to generate the output signal from the input signal by translating the frequency (and perhaps other characteristics) of the input signal to the frequency (and perhaps other characteristics) of the output signal.

[0069] An example embodiment of the UFT module 103 is generally illustrated in FIG. 1B. Generally, the UFT module 103 includes a switch 106 controlled by a control signal 108. The switch 106 is said to be a controlled switch.

[0070] As noted above, some UFT embodiments include other than three ports. For example, and without limitation, FIG. 2 illustrates an example UFT module 202. The example UFT module 202 includes a diode 204 having two ports, designated as Port 1 and Port 2/3. This embodiment does not include a third port, as indicated by the dotted line around the "Port 3" label. Other embodiments, as described herein, have more than three ports.

[0071] The UFT module is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications.

[0072] For example, a UFT module 115 can be used in a universal frequency down-conversion (UFD) module 114, an example of which is shown in FIG. 1C. In this capacity, the UFT module 115 frequency down-converts an input signal to an output signal.

[0073] As another example, as shown in FIG. 1D, a UFT module 117 can be used in a universal frequency up-conversion (UFU) module 116. In this capacity, the UFT module 117 frequency up-converts an input signal to an output signal.

[0074] These and other applications of the UFT module are described below. Additional applications of the UFT module will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. In some applications, the UFT module is a required component. In other applications, the UFT module is an optional component.

2.1 Frequency Down-Conversion

[0075] The present invention is directed to systems and methods of universal frequency down-conversion, and applications of same.

[0076] In particular, the following discussion describes down-converting using a Universal Frequency Translation Module. The down-conversion of an EM signal by aliasing the EM signal at an aliasing rate is fully described in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals," the full disclosure of which is incorporated herein by reference. A relevant portion of the above-mentioned patent is summarized below to describe down-converting an input signal to produce a down-converted signal that exists at a lower frequency or a baseband signal. The frequency translation aspects of the invention are further described in other documents referenced above, such as Application Ser. No. 09/550,644, entitled "Method and System for Down-converting an Electromagnetic Signal, and Transforms for Same, and Aperture Relationships."

[0077] FIG. 3A illustrates an aliasing module 300 for down-conversion using a universal frequency translation (UFT) module 302 which down-converts an EM input signal 304. In particular embodiments, aliasing module 300 includes a switch 308 and a capacitor 310 (or integrator). (In embodiments, the UFT module is considered

to include the switch and integrator.) The electronic alignment of the circuit components is flexible. That is, in one implementation, the switch 308 is in series with input signal 304 and capacitor 310 is shunted to ground (although it may be other than ground in configurations such as differential mode). In a second implementation (see FIG. 3G), the capacitor 310 is in series with the input signal 304 and the switch 308 is shunted to ground (although it may be other than ground in configurations such as differential mode). Aliasing module 300 with UFT module 302 can be tailored to down-convert a wide variety of electromagnetic signals using aliasing frequencies that are well below the frequencies of the EM input signal 304.

[0078] In one implementation, aliasing module 300 down-converts the input signal 304 to an intermediate frequency (IF) signal. In another implementation, the aliasing module 300 down-converts the input signal 304 to a demodulated baseband signal. In yet another implementation, the input signal 304 is a frequency modulated (FM) signal, and the aliasing module 300 down-converts it to a non-FM signal, such as a phase modulated (PM) signal or an amplitude modulated (AM) signal. Each of the above implementations is described below.

[0079] In an embodiment, the control signal 306 includes a train of pulses that repeat at an aliasing rate that is equal to, or less than, twice the frequency of the input signal 304. In this embodiment, the control signal 306 is referred to herein as an aliasing signal because it is below the Nyquist rate for the frequency of the input signal 304. Preferably, the frequency of control signal 306 is much less than the input signal 304.

[0080] A train of pulses 318 as shown in FIG. 3D controls the switch 308 to alias the input signal 304 with the control signal 306 to generate a down-converted output signal 312. More specifically, in an embodiment, switch 308 closes on a first edge of each pulse 320 of FIG. 3D and opens on a second edge of each pulse. When the switch 308 is closed, the input signal 304 is coupled to the capacitor 310, and charge is transferred from the input signal to the capacitor 310. The charge stored during successive pulses forms down-converted output signal 312.

[0081] Exemplary waveforms are shown in FIGs. 3B-3F.

[0082] FIG. 3B illustrates an analog amplitude modulated (AM) carrier signal 314 that is an example of input signal 304. For illustrative purposes, in FIG. 3C, an analog AM carrier signal portion 316 illustrates a portion of the analog AM carrier signal 314 on an expanded time scale. The analog AM carrier signal portion 316 illustrates the analog AM carrier signal 314 from time t_0 to time t_1.

[0083] FIG. 3D illustrates an exemplary aliasing signal 318 that is an example of control signal 306. Aliasing signal 318 is on approximately the same time scale as the analog AM carrier signal portion 316. In the example shown in FIG. 3D, the aliasing signal 318 includes a train of pulses 320 having negligible apertures that tend towards zero (the invention is not limited to this embodiment, as discussed below). The pulse aperture may also be referred to as the pulse width as will be understood by those skilled in the art(s). The pulses 320 repeat at an aliasing rate, or pulse repetition rate of aliasing signal 318. The aliasing rate is determined as described below.

[0084] As noted above, the train of pulses 320 (i.e., control signal 306) control the switch 308 to alias the analog AM carrier signal 316 (i.e., input signal 304) at the aliasing rate of the aliasing signal 318. Specifically, in this embodiment, the switch 308 closes on a first edge of each pulse and opens on a second edge of each pulse. When the switch 308 is closed, input signal 304 is coupled to the capacitor 310, and charge is transferred from the input signal 304 to the capacitor 310. The charge transferred during a pulse is referred to herein as an under-sample. Exemplary under-samples 322 form down-converted signal portion 324 (FIG. 3E) that corresponds to the analog AM carrier signal portion 316 (FIG. 3C) and the train of pulses 320 (FIG. 3D). The charge stored during successive under-samples of AM carrier signal 314 form the down-converted signal 324 (FIG. 3E) that is an example of down-converted output signal 312 (FIG. 3A). In FIG. 3F, a demodulated baseband signal 326 represents the demodulated baseband signal 324 after filtering on a compressed time

scale. As illustrated, down-converted signal 326 has substantially the same "amplitude envelope" as AM carrier signal 314. Therefore, FIGs. 3B-3F illustrate down-conversion of AM carrier signal 314.

[0085] The waveforms shown in FIGs. 3B-3F are discussed herein for illustrative purposes only, and are not limiting.

[0086] The aliasing rate of control signal 306 determines whether the input signal 304 is down-converted to an IF signal, down-converted to a demodulated baseband signal, or down-converted from an FM signal to a PM or an AM signal. Generally, relationships between the input signal 304, the aliasing rate of the control signal 306, and the down-converted output signal 312 are illustrated below:

$$\text{(Freq. of input signal 304)} = n \cdot \text{(Freq. of control signal 306)} \pm \text{(Freq. of down-converted output signal 312)}$$

For the examples contained herein, only the "+" condition will be discussed. Example values of n include, but are not limited to, n = {0.5, 1, 2, 3, 4, . . .}.

[0087] When the aliasing rate of control signal 306 is off-set from the frequency of input signal 304, or off-set from a harmonic or sub-harmonic thereof, input signal 304 is down-converted to an IF signal. This is because the under-sampling pulses occur at different phases of subsequent cycles of input signal 304. As a result, the under-samples form a lower frequency oscillating pattern. If the input signal 304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the down-converted IF signal. For example, to down-convert a 901 MHZ input signal to a 1 MHZ IF signal, the frequency of the control signal 306 would be calculated as follows:

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$

(901 MHZ - 1 MHZ)/n = 900/n

For n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 would be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

[0088] Alternatively, when the aliasing rate of the control signal 306 is substantially equal to the frequency of the input signal 304, or substantially equal to a harmonic or sub-harmonic thereof, input signal 304 is directly down-converted to a demodulated baseband signal. This is because, without modulation, the under-sampling pulses occur at the same point of subsequent cycles of the input signal 304. As a result, the under-samples form a constant output baseband signal. If the input signal 304 includes lower frequency changes, such as amplitude, frequency, phase, etc., or any combination thereof, the charge stored during associated under-samples reflects the lower frequency changes, resulting in similar changes on the demodulated baseband signal. For example, to directly down-convert a 900 MHZ input signal to a demodulated baseband signal (i.e., zero IF), the frequency of the control signal 306 would be calculated as follows:

$$(Freq_{input} - Freq_{IF})/n = Freq_{control}$$
$$(900\text{ MHZ} - 0\text{ MHZ})/n = 900\text{ MHZ}/n$$

For n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc.

[0089] Alternatively, to down-convert an input FM signal to a non-FM signal, a frequency within the FM bandwidth must be down-converted to baseband (i.e., zero IF). As an example, to down-convert a frequency shift keying (FSK) signal (a sub-set of FM) to a phase shift keying (PSK) signal (a subset of PM), the mid-point between a lower frequency F_1 and an upper frequency F_2 (that is, $[(F_1 + F_2) \div 2]$) of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal

having F_1 equal to 899 MHZ and F_2 equal to 901 MHZ, to a PSK signal, the aliasing rate of the control signal 306 would be calculated as follows:

$$\text{Frequency of the input} \quad = (F_1 + F_2) \div 2$$
$$= (899 \text{ MHZ} + 901 \text{ MHZ}) \div 2$$
$$= 900 \text{ MHZ}$$

Frequency of the down-converted signal = 0 (i.e., baseband)

$$(\text{Freq}_{\text{input}} - \text{Freq}_{\text{IF}})/n = \text{Freq}_{\text{control}}$$
$$(900 \text{ MHZ} - 0 \text{ MHZ})/n = 900 \text{ MHZ}/n$$

For n = {0.5, 1, 2, 3, 4 . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. The frequency of the down-converted PSK signal is substantially equal to one half the difference between the lower frequency F_1 and the upper frequency F_2.

[0090] As another example, to down-convert a FSK signal to an amplitude shift keying (ASK) signal (a subset of AM), either the lower frequency F_1 or the upper frequency F_2 of the FSK signal is down-converted to zero IF. For example, to down-convert an FSK signal having F_1 equal to 900 MHZ and F_2 equal to 901 MHZ, to an ASK signal, the aliasing rate of the control signal 306 should be substantially equal to:

$$(900 \text{ MHZ} - 0 \text{ MHZ})/n = 900 \text{ MHZ}/n, \text{ or}$$
$$(901 \text{ MHZ} - 0 \text{ MHZ})/n = 901 \text{ MHZ}/n.$$

For the former case of 900 MHZ/n, and for n = {0.5, 1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.8 GHz, 900 MHZ, 450 MHZ, 300 MHZ, 225 MHZ, etc. For the latter case of 901 MHZ/n, and for n = {0.5,

1, 2, 3, 4, . . .}, the frequency of the control signal 306 should be substantially equal to 1.802 GHz, 901 MHZ, 450.5 MHZ, 300.333 MHZ, 225.25 MHZ, etc. The frequency of the down-converted AM signal is substantially equal to the difference between the lower frequency F_1 and the upper frequency F_2 (i.e., 1 MHZ).

[0091] In an embodiment, the pulses of the control signal 306 have negligible apertures that tend towards zero. This makes the UFT module 302 a high input impedance device. This configuration is useful for situations where minimal disturbance of the input signal may be desired.

[0092] In another embodiment, the pulses of the control signal 306 have non-negligible apertures that tend away from zero. This makes the UFT module 302 a lower input impedance device. This allows the lower input impedance of the UFT module 302 to be substantially matched with a source impedance of the input signal 304. This also improves the energy transfer from the input signal 304 to the down-converted output signal 312, and hence the efficiency and signal to noise (s/n) ratio of UFT module 302.

[0093] Exemplary systems and methods for generating and optimizing the control signal 306 and for otherwise improving energy transfer and s/n ratio, are disclosed in U.S. Patent No. 6,061,551 entitled "Method and System for Down-Converting Electromagnetic Signals."

[0094] When the pulses of the control signal 306 have non-negligible apertures, the aliasing module 300 is referred to interchangeably herein as an energy transfer module or a gated transfer module, and the control signal 306 is referred to as an energy transfer signal. Exemplary systems and methods for generating and optimizing the control signal 306 and for otherwise improving energy transfer and/or signal to noise ratio in an energy transfer module are described below.

2.2 Optional Energy Transfer Signal Module

[0095] FIG. 4 illustrates an energy transfer system 401 that includes an optional energy transfer signal module 408, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 406.

[0096] In an embodiment, the optional energy transfer signal module 408 includes an aperture generator, an example of which is illustrated in FIG. 5 as an aperture generator 502. The aperture generator 502 generates non-negligible aperture pulses 508 from an input signal 412. The input signal 412 can be any type of periodic signal, including, but not limited to, a sinusoid, a square wave, a saw-tooth wave, etc. Systems for generating the input signal 412 are described below.

[0097] The width or aperture of the pulses 508 is determined by delay through the branch 506 of the aperture generator 502. Generally, as the desired pulse width increases, the difficulty in meeting the requirements of the aperture generator 502 decrease (i.e., the aperture generator is easier to implement). In other words, to generate non-negligible aperture pulses for a given EM input frequency, the components utilized in the example aperture generator 502 do not require reaction times as fast as those that are required in an under-sampling system operating with the same EM input frequency.

[0098] The example logic and implementation shown in the aperture generator 502 are provided for illustrative purposes only, and are not limiting. The actual logic employed can take many forms. The example aperture generator 502 includes an optional inverter 510, which is shown for polarity consistency with other examples provided herein.

[0099] An example implementation of the aperture generator 502 is illustrated in FIG. 6A. Additional examples of aperture generation logic are provided in FIGs. 7A and 7B. FIG. 7A illustrates a rising edge pulse generator 702, which generates pulses

508 on rising edges of the input signal 412. FIG. 7B illustrates a falling edge pulse generator 704, which generates pulses 508 on falling edges of the input signal 412. These circuits are provided for example only, and do not limit the invention.

[0100] In an embodiment, the input signal 412 is generated externally of the energy transfer signal module 408, as illustrated in FIG. 4. Alternatively, the input signal 412 is generated internally by the energy transfer signal module 408. The input signal 412 can be generated by an oscillator, as illustrated in FIG. 6B by an oscillator 602. The oscillator 602 can be internal to the energy transfer signal module 408 or external to the energy transfer signal module 408. The oscillator 602 can be external to the energy transfer system 401. The output of the oscillator 602 may be any periodic waveform.

[0101] The type of down-conversion performed by the energy transfer system 401 depends upon the aliasing rate of the energy transfer signal 406, which is determined by the frequency of the pulses 508. The frequency of the pulses 508 is determined by the frequency of the input signal 412.

[0102] The optional energy transfer signal module 408 can be implemented in hardware, software, firmware, or any combination thereof.

2.3 Impedance Matching

[0103] The example energy transfer module 300 described in reference to FIG. 3A, above, has input and output impedances generally defined by (1) the duty cycle of the switch module (i.e., UFT 302), and (2) the impedance of the storage module (e.g., capacitor 310), at the frequencies of interest (e.g. at the EM input, and intermediate/baseband frequencies).

[0104] Starting with an aperture width of approximately ½ the period of the EM signal being down-converted as an example embodiment, this aperture width (e.g. the "closed time") can be decreased (or increased). As the aperture width is

decreased, the characteristic impedance at the input and the output of the energy transfer module increases. Alternatively, as the aperture width increases from ½ the period of the EM signal being down-converted, the impedance of the energy transfer module decreases.

[0105] One of the steps in determining the characteristic input impedance of the energy transfer module could be to measure its value. In an embodiment, the energy transfer module's characteristic input impedance is 300 ohms. An impedance matching circuit can be utilized to efficiently couple an input EM signal that has a source impedance of, for example, 50 ohms, with the energy transfer module's impedance of, for example, 300 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary impedance directly or the use of an impedance match circuit as described below.

[0106] Referring to FIG. 8, a specific example embodiment using an RF signal as an input, assuming that the impedance 812 is a relatively low impedance of approximately 50 Ohms, for example, and the input impedance 816 is approximately 300 Ohms, an initial configuration for the input impedance match module 806 can include an inductor 906 and a capacitor 908, configured as shown in FIG. 9. The configuration of the inductor 906 and the capacitor 908 is a possible configuration when going from a low impedance to a high impedance. Inductor 906 and the capacitor 908 constitute an L match, the calculation of the values which is well known to those skilled in the relevant arts.

[0107] The output characteristic impedance can be impedance matched to take into consideration the desired output frequencies. One of the steps in determining the characteristic output impedance of the energy transfer module could be to measure its value. Balancing the very low impedance of the storage module at the input EM frequency, the storage module should have an impedance at the desired output frequencies that is preferably greater than or equal to the load that is intended to be driven (for example, in an embodiment, storage module impedance at a desired

1MHz output frequency is 2K ohm and the desired load to be driven is 50 ohms). An additional benefit of impedance matching is that filtering of unwanted signals can also be accomplished with the same components.

[0108] In an embodiment, the energy transfer module's characteristic output impedance is 2K ohms. An impedance matching circuit can be utilized to efficiently couple the down-converted signal with an output impedance of, for example, 2K ohms, to a load of, for example, 50 ohms. Matching these impedances can be accomplished in various manners, including providing the necessary load impedance directly or the use of an impedance match circuit as described below.

[0109] When matching from a high impedance to a low impedance, a capacitor 914 and an inductor 916 can be configured as shown in FIG. 9. The capacitor 914 and the inductor 916 constitute an L match, the calculation of the component values being well known to those skilled in the relevant arts.

[0110] The configuration of the input impedance match module 806 and the output impedance match module 808 are considered in embodiments to be initial starting points for impedance matching, in accordance with embodiments of the present invention. In some situations, the initial designs may be suitable without further optimization. In other situations, the initial designs can be enhanced in accordance with other various design criteria and considerations.

[0111] As other optional optimizing structures and/or components are utilized, their affect on the characteristic impedance of the energy transfer module should be taken into account in the match along with their own original criteria.

2.4 Frequency Up-Conversion

[0112] The present invention is directed to systems and methods of frequency up-conversion, and applications of same.

[0113] An example frequency up-conversion system 1000 is illustrated in FIG. 10. The frequency up-conversion system 1000 is now described.

[0114] An input signal 1002 (designated as "Control Signal" in FIG. 10) is accepted by a switch module 1004. For purposes of example only, assume that the input signal 1002 is a FM input signal 1306, an example of which is shown in FIG. 13C. FM input signal 1306 may have been generated by modulating information signal 1302 onto oscillating signal 1304 (FIGs. 13A and 13B). It should be understood that the invention is not limited to this embodiment. The information signal 1302 can be analog, digital, or any combination thereof, and any modulation scheme can be used.

[0115] The output of switch module 1004 is a harmonically rich signal 1006, shown for example in FIG. 13D as a harmonically rich signal 1308. The harmonically rich signal 1308 has a continuous and periodic waveform.

[0116] FIG. 13E is an expanded view of two sections of harmonically rich signal 1308, section 1310 and section 1312. The harmonically rich signal 1308 may be a rectangular wave, such as a square wave or a pulse (although, the invention is not limited to this embodiment). For ease of discussion, the term "rectangular waveform" is used to refer to waveforms that are substantially rectangular. In a similar manner, the term "square wave" refers to those waveforms that are substantially square and it is not the intent of the present invention that a perfect square wave be generated or needed.

[0117] Harmonically rich signal 1308 is comprised of a plurality of sinusoidal waves whose frequencies are integer multiples of the fundamental frequency of the waveform of the harmonically rich signal 1308. These sinusoidal waves are referred to as the harmonics of the underlying waveform, and the fundamental frequency is referred to as the first harmonic. FIG. 13F and FIG. 13G show separately the sinusoidal components making up the first, third, and fifth harmonics of section 1310 and section 1312. (Note that in theory there may be an infinite number of harmonics; in this example, because harmonically rich signal 1308 is shown as a square wave,

there are only odd harmonics). Three harmonics are shown simultaneously (but not summed) in FIG. 13H.

[0118] The relative amplitudes of the harmonics are generally a function of the relative widths of the pulses of harmonically rich signal 1006 and the period of the fundamental frequency, and can be determined by doing a Fourier analysis of harmonically rich signal 1006. According to an embodiment of the invention, the input signal 1306 may be shaped to ensure that the amplitude of the desired harmonic is sufficient for its intended use (e.g., transmission).

[0119] An optional filter 1008 filters out any undesired frequencies (harmonics), and outputs an electromagnetic (EM) signal at the desired harmonic frequency or frequencies as an output signal 1010, shown for example as a filtered output signal 1314 in FIG. 13I.

[0120] FIG. 11 illustrates an example universal frequency up-conversion (UFU) module 1101. The UFU module 1101 includes an example switch module 1004, which comprises a bias signal 1102, a resistor or impedance 1104, a universal frequency translator (UFT) 1150, and a ground 1108. The UFT 1150 includes a switch 1106. The input signal 1002 (designated as "Control Signal" in FIG. 11) controls the switch 1106 in the UFT 1150, and causes it to close and open. Harmonically rich signal 1006 is generated at a node 1105 located between the resistor or impedance 1104 and the switch 1106.

[0121] Also in FIG. 11, it can be seen that an example optional filter 1008 is comprised of a capacitor 1110 and an inductor 1112 shunted to a ground 1114. The filter is designed to filter out the undesired harmonics of harmonically rich signal 1006.

[0122] The invention is not limited to the UFU embodiment shown in FIG. 11. For example, in an alternate embodiment shown in FIG. 12, an unshaped input signal 1201 is routed to a pulse shaping module 1202. The pulse shaping module 1202 modifies the unshaped input signal 1201 to generate a (modified) input signal 1002

(designated as the "Control Signal" in FIG. 12). The input signal 1002 is routed to the switch module 1004, which operates in the manner described above. Also, the filter 1008 of FIG. 12 operates in the manner described above.

[0123] The purpose of the pulse shaping module 1202 is to define the pulse width of the input signal 1002. Recall that the input signal 1002 controls the opening and closing of the switch 1106 in switch module 1004. During such operation, the pulse width of the input signal 1002 establishes the pulse width of the harmonically rich signal 1006. As stated above, the relative amplitudes of the harmonics of the harmonically rich signal 1006 are a function of at least the pulse width of the harmonically rich signal 1006. As such, the pulse width of the input signal 1002 contributes to setting the relative amplitudes of the harmonics of harmonically rich signal 1006.

[0124] Further details of up-conversion as described in this section are presented in U.S. Patent No. 6,091,940, entitled "Method and System for Frequency Up-Conversion," incorporated herein by reference in its entirety.

2.5 Enhanced Signal Reception

[0125] The present invention is directed to systems and methods of enhanced signal reception (ESR), and applications of same, which are described in the above-referenced U.S. Patent No. 6,061,555, entitled "Method and System for Ensuring Reception of a Communications Signal," incorporated herein by reference in its entirety.

2.6 Unified Down-Conversion and Filtering

[0126] The present invention is directed to systems and methods of unified down-conversion and filtering (UDF), and applications of same.

[0127] In particular, the present invention includes a unified down-converting and filtering (UDF) module that performs frequency selectivity and frequency translation in a unified (i.e., integrated) manner. By operating in this manner, the invention achieves high frequency selectivity prior to frequency translation (the invention is not limited to this embodiment). The invention achieves high frequency selectivity at substantially any frequency, including but not limited to RF (radio frequency) and greater frequencies. It should be understood that the invention is not limited to this example of RF and greater frequencies. The invention is intended, adapted, and capable of working with lower than radio frequencies.

[0128] FIG. 14 is a conceptual block diagram of a UDF module 1402 according to an embodiment of the present invention. The UDF module 1402 performs at least frequency translation and frequency selectivity.

[0129] The effect achieved by the UDF module 1402 is to perform the frequency selectivity operation prior to the performance of the frequency translation operation. Thus, the UDF module 1402 effectively performs input filtering.

[0130] According to embodiments of the present invention, such input filtering involves a relatively narrow bandwidth. For example, such input filtering may represent channel select filtering, where the filter bandwidth may be, for example, 50 KHz to 150 KHz. It should be understood, however, that the invention is not limited to these frequencies. The invention is intended, adapted, and capable of achieving filter bandwidths of less than and greater than these values.

[0131] In embodiments of the invention, input signals 1404 received by the UDF module 1402 are at radio frequencies. The UDF module 1402 effectively operates to input filter these RF input signals 1404. Specifically, in these embodiments, the UDF module 1402 effectively performs input, channel select filtering of the RF input signal 1404. Accordingly, the invention achieves high selectivity at high frequencies.

[0132] The UDF module 1402 effectively performs various types of filtering, including but not limited to bandpass filtering, low pass filtering, high pass filtering, notch filtering, all pass filtering, band stop filtering, etc., and combinations thereof.

[0133] Conceptually, the UDF module 1402 includes a frequency translator 1408. The frequency translator 1408 conceptually represents that portion of the UDF module 1402 that performs frequency translation (down conversion).

[0134] The UDF module 1402 also conceptually includes an apparent input filter 1406 (also sometimes called an input filtering emulator). Conceptually, the apparent input filter 1406 represents that portion of the UDF module 1402 that performs input filtering.

[0135] In practice, the input filtering operation performed by the UDF module 1402 is integrated with the frequency translation operation. The input filtering operation can be viewed as being performed concurrently with the frequency translation operation. This is a reason why the input filter 1406 is herein referred to as an "apparent" input filter 1406.

[0136] The UDF module 1402 of the present invention includes a number of advantages. For example, high selectivity at high frequencies is realizable using the UDF module 1402. This feature of the invention is evident by the high Q factors that are attainable. For example, and without limitation, the UDF module 1402 can be designed with a filter center frequency f_C on the order of 900 MHZ, and a filter bandwidth on the order of 50 KHz. This represents a Q of 18,000 (Q is equal to the center frequency divided by the bandwidth).

[0137] It should be understood that the invention is not limited to filters with high Q factors. The filters contemplated by the present invention may have lesser or greater Qs, depending on the application, design, and/or implementation. Also, the scope of the invention includes filters where Q factor as discussed herein is not applicable.

[0138] The invention exhibits additional advantages. For example, the filtering center frequency f_C of the UDF module 1402 can be electrically adjusted, either statically or dynamically.

[0139] Also, the UDF module 1402 can be designed to amplify input signals.

[0140] Further, the UDF module 1402 can be implemented without large resistors, capacitors, or inductors. Also, the UDF module 1402 does not require that tight tolerances be maintained on the values of its individual components, i.e., its resistors, capacitors, inductors, etc. As a result, the architecture of the UDF module 1402 is friendly to integrated circuit design techniques and processes.

[0141] The features and advantages exhibited by the UDF module 1402 are achieved at least in part by adopting a new technological paradigm with respect to frequency selectivity and translation. Specifically, according to the present invention, the UDF module 1402 performs the frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation. According to the invention, operations relating to frequency translation also contribute to the performance of frequency selectivity, and vice versa.

[0142] According to embodiments of the present invention, the UDF module generates an output signal from an input signal using samples/instances of the input signal and/or samples/instances of the output signal.

[0143] More particularly, first, the input signal is under-sampled. This input sample includes information (such as amplitude, phase, etc.) representative of the input signal existing at the time the sample was taken.

[0144] As described further below, the effect of repetitively performing this step is to translate the frequency (that is, down-convert) of the input signal to a desired lower frequency, such as an intermediate frequency (IF) or baseband.

[0145] Next, the input sample is held (that is, delayed).

[0146] Then, one or more delayed input samples (some of which may have been scaled) are combined with one or more delayed instances of the output signal (some of which may have been scaled) to generate a current instance of the output signal.

[0147] Thus, according to a preferred embodiment of the invention, the output signal is generated from prior samples/instances of the input signal and/or the output signal. (It is noted that, in some embodiments of the invention, current samples/instances of the input signal and/or the output signal may be used to generate current instances of the output signal.). By operating in this manner, the UDF module 1402 preferably performs input filtering and frequency down-conversion in a unified manner.

[0148] Further details of unified down-conversion and filtering as described in this section are presented in U.S. Patent No. 6,049,706, entitled "Integrated Frequency Translation And Selectivity," filed October 21, 1998, and incorporated herein by reference in its entirety.

3. Example Down-Converter Embodiments of the Invention

[0149] As noted above, the UFT module of the present invention is a very powerful and flexible device. Its flexibility is illustrated, in part, by the wide range of applications and combinations in which it can be used. Its power is illustrated, in part, by the usefulness and performance of such applications and combinations.

[0150] Such applications and combinations include, for example and without limitation, applications/combinations comprising and/or involving one or more of: (1) frequency translation; (2) frequency down-conversion; (3) frequency up-conversion; (4) receiving; (5) transmitting; (6) filtering; and/or (7) signal transmission and reception in environments containing potentially jamming signals. Example receiver, transmitter, and transceiver embodiments implemented using the UFT module of the present invention are set forth below.

3.1 Receiver Embodiments

[0151] In embodiments, a receiver according to the invention includes an aliasing module for down-conversion that uses a universal frequency translation (UFT) module to down-convert an EM input signal. For example, in embodiments, the receiver includes the aliasing module 300 described above, in reference to FIG. 3A or FIG. 3G. As described in more detail above, the aliasing module 300 may be used to down-convert an EM input signal to an intermediate frequency (IF) signal or a demodulated baseband signal.

[0152] In alternate embodiments, the receiver may include the energy transfer system 401, including energy transfer module 404, described above, in reference to FIG. 4. As described in more detail above, the energy transfer system 401 may be used to down-convert an EM signal to an intermediate frequency (IF) signal or a demodulated baseband signal. As also described above, the aliasing module 300 or the energy transfer system 401 may include an optional energy transfer signal module 408, which can perform any of a variety of functions or combinations of functions including, but not limited to, generating the energy transfer signal 406 of various aperture widths.

[0153] In further embodiments of the present invention, the receiver may include the impedance matching circuits and/or techniques described herein for enhancing the energy transfer system of the receiver.

3.1.1 In-Phase/Quadrature-Phase (I/Q) Modulation Mode Receiver Embodiments

[0154] FIG. 15 illustrates an exemplary I/Q modulation mode embodiment of a receiver 1502, according to an embodiment of the present invention. This I/Q modulation mode embodiment is described herein for purposes of illustration, and

not limitation. Alternate I/Q modulation mode embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein), as well as embodiments of other modulation modes, will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0155] Receiver 1502 comprises an I/Q modulation mode receiver 1538, a first optional amplifier 1516, a first optional filter 1518, a second optional amplifier 1520, and a second optional filter 1522.

[0156] I/Q modulation mode receiver 1538 comprises an oscillator 1506, a first UFD module 1508, a second UFD module 1510, a first UFT module 1512, a second UFT module 1514, and a phase shifter 1524.

[0157] Oscillator 1506 provides an oscillating signal used by both first UFD module 1508 and second UFD module 1510 via the phase shifter 1524. Oscillator 1506 generates an "I" oscillating signal 1526.

[0158] "I" oscillating signal 1526 is input to first UFD module 1508. First UFD module 1508 comprises at least one UFT module 1512. First UFD module 1508 frequency down-converts and demodulates received signal 1504 to down-converted "I" signal 1530 according to "I" oscillating signal 1526.

[0159] Phase shifter 1524 receives "I" oscillating signal 1526, and outputs "Q" oscillating signal 1528, which is a replica of "I" oscillating signal 1526 shifted preferably by 90 degrees.

[0160] Second UFD module 1510 inputs "Q" oscillating signal 1528. Second UFD module 1510 comprises at least one UFT module 1514. Second UFD module 1510 frequency down-converts and demodulates received signal 1504 to down-converted "Q" signal 1532 according to "Q" oscillating signal 1528.

[0161] Down-converted "I" signal 1530 is optionally amplified by first optional amplifier 1516 and optionally filtered by first optional filter 1518, and a first information output signal 1534 is output.

[0162] Down-converted "Q" signal 1532 is optionally amplified by second optional amplifier 1520 and optionally filtered by second optional filter 1522, and a second information output signal 1536 is output.

[0163] In the embodiment depicted in FIG. 15, first information output signal 1534 and second information output signal 1536 comprise a down-converted baseband signal. In embodiments, first information output signal 1534 and second information output signal 1536 are individually received and processed by related system components. Alternatively, first information output signal 1534 and second information output signal 1536 are recombined into a single signal before being received and processed by related system components.

[0164] Alternate configurations for I/Q modulation mode receiver 1538 will be apparent to persons skilled in the relevant art(s) from the teachings herein. For instance, an alternate embodiment exists wherein phase shifter 1524 is coupled between received signal 1504 and UFD module 1510, instead of the configuration described above. This and other such I/Q modulation mode receiver embodiments will be apparent to persons skilled in the relevant art(s) based upon the teachings herein, and are within the scope of the present invention.

4. DC Offset and Circuit Gain Considerations and Corrections

[0165] Various embodiments related to the method(s) and structure(s) described herein are presented in this section (and its subsections). Exemplary WLAN receiver channel circuits are provided below, and circuits used to reduce or eliminate problems of DC offset in the WLAN receiver channel circuits are described. The embodiments of the present invention are applicable to any WLAN receiver circuit, such as IEEE 802.11 WLAN standard compliant receivers, including the IEEE 802.11a and 802.11b extensions, and to other communication standards.

[0166] These embodiments are described herein for purposes of illustration, and not

limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments. Furthermore, the invention is applicable to additional communication system environments. For instance, the invention as disclosed herein is applicable to any type of communication system receiver, such as wireless personal area network (WPAN) receivers (including the Bluetooth standard), wireless metropolitan area network (WMAN) receivers, code division multiple access (CDMA) receivers (including wideband CDMA receivers), Global System for Mobile Communications (GSM) standard compatible receivers, and 3rd Generation (3G) network receivers.

4.1 Overview of DC Offset

[0167] Receivers, and other electronic circuits, may suffer from problems of DC offset and re-radiation. Generally, "DC offset" refers to a DC voltage level that is added to a signal of interest by related circuitry. The related circuitry creates the DC offset voltage through a variety of mechanisms that are well known. Some of these mechanisms are discussed in further detail below. "Re-radiation" is an undesired phenomenon where an unwanted signal is generated by circuitry, such as by an oscillator, and is transmitted by an antenna. The unwanted signal may then be received by circuitry, to interfere with the signal of interest. Such re-radiation may also lead to unwanted DC offset voltages.

[0168] If a DC offset voltage value is significant, it can degrade the quality of the signal of interest. In a receiver, for example, the signal of interest may be a down-converted signal. Unless reduced or eliminated, the added DC offset voltage level may undesirably change the voltage value of the down-converted signal. As a result,

the desired voltage value of the down-converted signal may be difficult to ascertain by downstream processing.

[0169] For example, unwanted DC offset voltages created by receiver channel amplifiers may be inserted into the receiver channel signal path. FIG. 18 shows a DC offset voltage 1802 present in an example model of an operational amplifier gain stage. DC offset voltage 1802 is internally generated in operational amplifier 1804, and may be considered to be a voltage inserted between the amplifier inputs. Typically, DC offset voltage 1802 is a differential input voltage resulting from the mismatch of the input stages of operational amplifier 1804. Due to DC offset voltage 1802 (V_{IO}), an unwanted output voltage offset (V_{OO}) will appear in output voltage 1808. V_{IO} is amplified by the circuit closed loop gain to create V_{OO}. For example, in the configuration shown in FIG. 18, V_{OO} may be calculated according to the following equation:

$$V_{oo} = (\frac{R2}{R1} + 1)V_{IO}$$

This unwanted output DC offset voltage is input to subsequent amplifiers in the receiver channel and is accordingly amplified. If it becomes significant, it may cause outputs of the subsequent amplifiers to reach their voltage rails. In any event, DC offset voltages present in the receiver channel amplifiers may lead to an erroneous output signal.

[0170] Frequency down-converters may input DC offset voltages into the receiver channel. Embodiments of the UFT module may be used in many communications applications, including embodiments of the UFD module, to frequency down-convert signals in receivers. For some of these applications, the signal space may include waveforms with near DC content. Hence, it may be advantageous to limit the amount of artificial DC insertion or DC offsets contributed by the UFD module or

its complimentary demodulation architecture.

[0171] There are at least three significant categories of offsets related to operation of the UFD module, which are listed as follows:

1. Clock Excitation or Charge Injected
2. Re-radiation Offsets
3. Intermodulation Distortion

Each category possesses its own mechanisms. Further description of these categories of offsets in relation to the UFD module are provided in U.S. Serial No. 09/526,041, titled "DC Offset, Re-radiation, and I/Q Solutions Using Universal Frequency Translation Technology," filed March 14, 2000, the disclosure of which is incorporated by reference herein in its entirety. These sources of DC offset may lead to erroneous receiver channel output signals.

[0172] Example methods and systems are provided in the sub-sections below for reducing or eliminating unwanted DC offsets. Such methods and systems may be used separately, or in any combination, to address offset issues.

4.2 Exemplary Communications System Receiver Channel

[0173] FIG. 16 shows an exemplary receiver channel 1600 in which embodiments of the present invention may be implemented. Receiver channel 1600 may be used to receive WLAN signals, or other signal types.

[0174] Receiver channel 1600 includes an optional low noise amplifier 1602, a second automatic gain control (AGC) amplifier 1604, a down-converter 1606, a first optional amplifier/filter section 1608, a first AGC amplifier 1610, a second optional amplifier/filter section 1612, and an antenna 1614. The present invention is also applicable to further receiver channel embodiments than receiver channel 1600, with

fewer or more elements than shown in FIG. 16. Furthermore, the elements of receiver channel 1600 are not necessarily required to be arranged in the order shown in FIG. 16. For example, when first amplifier/filter section 1612 is present, some or all of it may be implemented upstream from down-converter 1606. Further embodiments for receiver channel 1600 will be apparent to persons skilled in the relevant art(s) from the teachings herein.

[0175] In an embodiment, more than one receiver channel 1600 may be required to receive a particular input signal. In the case of an I/Q modulated input signal, for example, a first receiver channel 1600 may be used to down-convert the I-channel, and a second receiver channel 1600 may be used to down-convert the Q-channel. Alternatively, for example, receiver channel 1600 may be divided into two channels (an I and Q channel) following LNA 1602 or second AGC amplifier 1604.

[0176] Antenna 1614 receives an input RF signal 1616. LNA 1602 (when present) receives and amplifies input RF signal 1616.

[0177] Second AGC amplifier 1604 receives input RF signal 1616 and receives a second AGC signal 1620. Second AGC amplifier 1604 amplifies input RF signal 1616 by an amount controlled by second AGC signal 1620, and outputs amplified RF signal 1618. Typically, second AGC signal 1620 is generated by downstream circuitry that detects the level of the receiver channel signal at a given location (not shown), and then determines by what amount the signal level of the receiver channel needs to be amplified, i.e., increased or decreased, to produce an acceptable receiver channel signal level.

[0178] Down-converter 1606 receives amplified RF signal 1618. Down-converter 1606 frequency down-converts, and optionally demodulates amplified input RF signal 1618 to a down-converted signal 1622. For example, in an embodiment, down-converter 1606 includes a conventional down-converter, such as a superheterodyne configuration. In another embodiment, down-converter 1606 may include a UFD module (e.g., UFD module 114 shown in FIG. 1C, aliasing module

300 shown in FIG. 3A) for frequency down-conversion/demodulation. Down-converted signal 1622 may be an intermediate frequency signal or baseband signal.

[0179] When present, first amplifier-filter section 1608 amplifies and/or filters down-converted signal 1622. First amplifier-filter section 1608 includes one or more amplifiers, such as operational amplifiers, and filter circuits for conditioning down-converted signal 1622. Any filter circuits that are present may have low-pass, high-pass, band-pass, and/or band-stop filter characteristics, for example. The filters may be active or passive filter types.

[0180] First AGC amplifier 1610 receives the optionally amplified/filtered down-converted signal 1622 and receives a first AGC signal 1626. First AGC amplifier 1610 amplifies down-converted signal 1622 by an amount controlled by first AGC signal 1626, and outputs amplified down-converted signal 1624. Similarly to second AGC signal 1620, first AGC signal 1626 is generated by circuitry that detects the level of the receiver channel signal at a given location (not shown), and then determines by what amount the signal level of the receiver channel needs to be amplified, i.e., increased or decreased, to produce an acceptable receiver channel signal level.

[0181] When present, second amplifier-filter section 1612 amplifies and/or filters amplified down-converted signal 1624. Second amplifier-filter section 1612 includes one or more amplifiers, such as operational amplifiers, and filter circuits for conditioning amplified down-converted signal 1624. Any filter circuits that are present may have low-pass, high-pass, band-pass, and/or band-stop filter characteristics, for example. The filters may be active or passive filter types. Second amplifier-filter section 1612 outputs an output signal 1628. Output signal 1628 may be an intermediate frequency signal that is passed on to further down-converters if needed, or a baseband signal that is passed to subsequent baseband signal processor circuitry.

[0182] Each element of receiver channel 1600 may introduce DC offsets, as

described above, into the signal passing through receiver channel 1600. The following subsections further describe some of these sources of DC offset, and describe embodiments of the present invention for reducing or eliminating unwanted DC offset in a receiver channel.

4.3 Embodiments for Cancellation of DC Offset by Closed Feedback Loop

[0183] As described above, DC offset voltages may be introduced by elements of a receiver channel. DC offset voltages due to a down-converter, such as a UFD module, are briefly described in section 4.1 above, as are DC offset voltages due to an operational amplifier. These DC offset voltages can lead to erroneous receiver channel output signals. Hence, it would be desirable to reduce or eliminate DC offset voltages due to these and other elements of the receiver channel.

[0184] FIG. 20 shows an exemplary high-pass filter, or differentiator circuit 2000 that may be used to reduce or eliminate DC offset voltages in a receiver channel. Circuit 2000 is located in series in the receiver channel path. Circuit 2000 includes an amplifier 2002, a first resistor 2004, a capacitor 2006, and a second resistor 2008. Amplifier 2002 receives receiver channel signal 2010. First resistor 2004 and capacitor 2006 are coupled in series between the output of amplifier 2002 and the circuit output, output signal 2012. Second resistor 2008 is coupled between output signal 2012 and a ground or other potential.

[0185] A transfer function for circuit 2000 is provided below, wherein amplifier 2002 has a gain of *G*:

$$\frac{Vo}{Vi} = \frac{G \bullet \dfrac{R2}{R1 + R2}}{1 + \dfrac{1}{(R1 + R2)C \bullet s}}$$

Circuit 2000 is suitable for correcting an instantaneous DC offset, but may not be efficient in correcting for DC offset voltages over an infinite amount of time. For example, when there are perturbations in the DC offset voltage due to the temperature drift of circuit components, potentials may form across capacitor 2006 that do not easily dissipate. Hence, circuit 2000 is not necessarily a desirable solution in all situations.

[0186] According to the present invention, DC offset voltages may be reduced or eliminated from a receiver channel using a closed feedback loop to subtract out the DC offset voltage. Embodiments for the closed feedback loop are provided as follows. These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

[0187] In embodiments, a DC offset voltage at a particular receiver channel node is measured. Using a feedback loop, the measured DC offset voltage is subtracted from the receiver channel. FIG. 19 shows an example feedback loop 1900 for reducing DC offset in a receiver channel, according to an embodiment of the present invention. Feedback loop 1900 includes an optional first amplifier 1902, an integrator 1904, a summing node 1906, and a second amplifier 1908. Feedback loop 1900 may be located at any point in a receiver channel, including at RF, IF, and baseband portions of the receiver channel. The direction of signal flow in the receiver channel is shown by arrow 1910.

[0188] Feedback loop 1900 provides a more robust approach to removing DC offset than circuit 2000, described above and shown in FIG. 20. Feedback loop 1900 continually measures the DC level of the receiver channel node, and continually corrects for it. Furthermore, feedback loop 1900 allows for rapid acquisition and removal of DC offset voltages.

[0189] The receiver channel DC offset is monitored at an output node 1914. Output node 1914 is located in the receiver channel signal path. Output node 1914 also provides an output signal 1916 of feedback loop 1900. Output signal 1916 is further coupled to subsequent components of the receiver channel.

[0190] Integrator 1904 has an input coupled to output node 1914 through first amplifier 1902. First amplifier 1902 is optional, and when first amplifier 1902 is not present, integrator 1904 may be directly coupled to output node 1914. Integrator 1904 integrates the signal received from output node 1914, which includes a DC offset voltage. Integrator 1904 outputs an integrator output signal 1918. Integrator 1904 may include passive and/or active circuit elements to provide the integration function.

[0191] Summing node 1906 is located in the receiver channel upstream from output node 1914. A receiver channel signal 1912 is coupled as a first input to summing node 1906. The output of integrator 1904, integrator output signal 1918, is coupled as a second input to summing node 1906.

[0192] Summing node 1906 may be merely a signal node in the receiver channel, or may include circuit components (active and/or passive) for combining integrator output signal 1918 and receiver channel signal 1912. Integrator output signal 1918 includes the DC offset to be removed from the receiver channel that is determined by feedback loop 1900. Integrator output signal 1918 may be inverted, such that summing node 1906 adds integrator output signal 1918 and receiver channel signal 1912, or may be non-inverted, so that summing node 1906 subtracts integrator output signal 1918 from receiver channel signal 1912. For example, integrator 1904 may

be configured as an inverting integrator, or first amplifier 1902, when present, may be configured as an inverting amplifier, so that integrator output signal 1918 is inverted.

[0193] One or more amplifiers and other circuit components may be coupled between summing node 1906 and output node 1914. Feedback loop 1900 operates to eliminate or reduce DC offsets produced by these circuit components from the receiver channel, so that they do not substantially appear in output signal 1916. In the example embodiment shown in FIG.19, second amplifier 1908 is coupled between summing node 1906 and output node 1914, and may provide a DC offset voltage at output node 1914.

[0194] FIG. 21 shows an example embodiment for integrator 1904, including an operational amplifier 2102, a resistor 2104, and a capacitor 2106 that are configured in an integrating amplifier configuration. Integrator input signal 1920 is coupled to a first terminal of resistor 2104. A second terminal of resistor 2104 is coupled to a first input 2112 of amplifier 2102. A second input 2114 of amplifier 2102 is coupled to ground or other reference potential. Capacitor 2106 is coupled between first input 2112 and output 2116 of amplifier 2102. Output 2116 is coupled to integrator output signal 1918.

[0195] Integrator 1904 shown in FIG. 21 performs the integration operation of:

$$v_o(t) = -\frac{1}{CR}\int_0^t v_i(t)\,dt$$

$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$

Hence, as indicated by the minus sign in the integrator transfer function, integrator 1904 is an inverting integrator. FIG. 24A shows a frequency response 2400 of an ideal integrator similar in an embodiment to integrator 1904. The integrator

frequency response 2400 of FIG. 24A has a time constant, CR, determined by the values of capacitor 2106 and resistor 2104.

[0196] The transfer function for feedback loop 1900 shown in FIG. 19 may be calculated as follows:

$$V_o(s) = (K_i G_{fb} V_o(s) + V_i(s))G$$

$$V_o(1 - K_i G_{fb} G) = V_i G$$

$$\frac{V_o}{V_i} = \frac{V_i G}{1 - K_i G_{fb} G} = \frac{G}{1 + \dfrac{G_{fb} G}{RCs}} = \frac{Gs}{s + \dfrac{G_{fb} G}{RC}}$$

where: $K_i = 1/RCs$

G = the gain of second amplifier 1908,

G_{fb} = the loop gain/gain of first amplifier 1902,

V_o = output signal 1916, and

V_i = receiver channel signal 1912.

FIG. 24B shows a plot of the transfer function of feedback loop 1900. Feedback loop 1900 is useful for reducing or eliminating DC offset voltages originating between summing node 1906 and output node 1914 in the receiver channel, in addition to DC offset voltages existing in receiver channel signal 1912. For example, a DC offset voltage of second amplifier 1908, V_{IOA}, appearing at the input of second amplifier 1908, is reduced as follows:

$$V_o(s) = (K_i G_{fb} V_o(s) + V_i(s) + V_{IOA})G$$

$$V_o(1 - K_i G_{fb} G) = V_{IOA} G \quad \text{where } V_i = 0$$

$$V_o = \frac{V_{IOA} G}{1 - K_i G_{fb} G}$$

For large loop gain G_{fb}

$$|V_o| \approx \frac{V_{IOA}}{K_i G_{fb}}$$

In some situations, DC offset voltages appearing in the feedback path of feedback loop 1900 may not be reduced as effectively. For example, FIG. 22 shows an embodiment of feedback loop 1900, where first amplifier 1902 is divided into a first feedback amplifier 2202 and a second feedback amplifier 2204, according to an embodiment of the present invention. FIG. 22 shows a DC offset voltage of integrator 1904, V_{IOI}, being added to the feedback signal path at the input of integrator 1904. V_{IOI} affects output signal 1916 as follows:

$$V_o = (K_i G_{fb1} V_o + K_i V_{IOI}) G_{fb2} \bullet G + V_i G$$

Where $G_{fb} = G_{fb1} G_{fb2}$

$$V_o = \frac{G K_i G_{fb2} V_{IOI}}{1 - G K_i G_{fb}} + V_i \frac{G}{1 - G K_i G_{fb}}$$

For $V_i = 0$ and large loop gain G_{fb},

$$|V_o| \approx \frac{V_{IOI}}{G_{fb1}}$$

Hence, in the embodiment of FIG. 22, the DC offset contribution of integrator 1904, V_{IOI}, can be reduced by increasing the gain of first feedback amplifier 2202 (with a

corresponding decrease in the gain of second feedback amplifier 2204 to keep from affecting the overall loop gain).

[0197] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0198] As described above, the frequency response of the feedback loop may be varied. The varying of the frequency response of the feedback loop is described more fully in the next sub-section. Examples of the operation of closed feedback loop embodiments of the present invention are then described in the following sub-section.

4.3.1 Variable Frequency Response Embodiments of the Present Invention

[0199] In some communication system receivers, it may be advantageous to incorporate a feedback loop 1900 with a variable frequency response. This may allow for DC offset voltages to be acquired according to different degrees of accuracy, while allowing the receiver channel to better pass signals of different signal formats. By varying the frequency response of feedback loop 1900, a frequency response of the receiver channel may be correspondingly varied. Furthermore, the ability to vary the frequency response of feedback loop 1900 allows for more rapid acquisition of DC offset voltages.

[0200] For example, a frequency response with a high-pass filter characteristic may be desirable to avoid problems of 1/f noise, also known as "flicker" noise. 1/f noise is produced by amplifiers, and gets its name from the fact that its characteristic curve has a slope close to 1/f. 1/f noise can cause subsequent amplifiers in the receiver

channel to saturate, and can otherwise interfere with the receiver channel signal. Hence, it may be advantageous to have a high-pass filter characteristic in the receiver frequency response to avoid 1/f noise. FIG. 40 shows an example 1/f noise characteristic curve 4002. The 1/f corner frequency for an amplifier can be around 10 KHz, or even greater, as shown in 1/f noise characteristic curve 4002. The noise level to the left of the 1/f corner frequency can be in the microvolts. Hence, a high-pass corner frequency of 100 KHz or 1 MHz may be desirable, for example.

[0201] However, a signal packet being received may have characteristics making a lower high-pass filter corner frequency more desirable. For example, in a 802.11 standard WLAN environment, a CCK modulated data portion of a WLAN signal frame may have this characteristic, as opposed to the WLAN signal frame preamble which may not. Furthermore, it may be advantageous to have a lower high-pass filter corner frequency in order to better capture and follow DC offset voltage changes due to thermal drift, etc. These considerations must be balanced with the problem of 1/f noise.

[0202] In a WLAN (or other) communication system receiver, two or more separately located antennas may be used. During signal acquisition, the antennas may be sequentially switched on, so that each antenna is individually coupled to the same receiver channel. This antenna "diversity" switch allows for the antennas to be sequenced through, until it is determined which antenna allows for the strongest received signal. During this period of diversity antenna switching, a first frequency response for feedback loop 1900 may be desired, due to potentially a higher or lower tolerance in the acceptability of DC offset. Once an antenna has been selected, further frequency responses for feedback loop 1900 may be desired, due to changes in the tolerance for DC offset. Different frequency responses for feedback loop 1900 may be desirable when down-converting each of the preamble and data portions of a data frame, for example.

[0203] Hence, in an embodiment of the present invention, the frequency response of

feedback loop 1900 is variable. The frequency response of feedback loop 1900 may be varied by changing component values in the feedback loop circuit, for example.

[0204] In an embodiment, integrator 1904 in feedback loop 1900 may be variable. The frequency response of integrator 1904 may be made variable by varying its respective components. Furthermore, integrator 1904 may receive one or more control signals to control the timing of frequency response changes for integrator 1904. FIG. 51 shows an block diagram of integrator 1904, according to an embodiment of the present invention. As shown in FIG. 51, integrator 1904 may receive a control signal 5102. One or more components of integrator 1904 may be varied in response to control signal 5102. In the embodiment of integrator 1904 shown in FIG. 21, the values of resistor 2104 and/or capacitor 2106 may be made variable in response to a control signal in order to vary the frequency response of integrator 1904. Other components may be made variable in other embodiments for integrator 1904.

[0205] FIG. 23 shows an integrator 1904, where resistor 2104 is a variable resistor, according to an embodiment of the present invention. Integrator 1904 as shown in FIG. 23 is configured substantially similarly to integrator 1904 shown in FIG. 21, with resistor 2104 divided into a first resistor 2302, a second resistor 2304, and a third resistor 2306, which are coupled in series. Furthermore, as shown in FIG. 23, integrator 1904 receives two control signals, first and second control signals 2312 and 2314.

[0206] A first switch 2308 is coupled across second resistor 2304, and receives a first control signal 2312. A second switch 2310 is coupled across third resistor 2306, and receives a second control signal 2314. By using first control signal 2312 and second control signal 2314 to switch second resistor 2304 and third resistor 2306 in and out of the circuit of integrator 1904, the frequency response of integrator 1904 may be varied. Any number of one or more resistors with corresponding switches in parallel may be used, according to the present invention, each providing for a corresponding

change in the frequency response for integrator 1904.

[0207] In an example embodiment, first and second control signals 2312 and 2314 are sequenced between three consecutive time periods according to the following table:

	first control signal 2312	second control signal 2314
first time period	1	1
second time period	0	1
third time period	0	0

Table 1

Due to the sequencing shown in Table 1, during the first time period, second and third resistors 2304 and 2306 are both shorted out of resistor 2104. First and second controls signals 2312 and 2314 (which are both high) open both of first and second switches 2308 and 2310, respectively. Only first resistor 2302 has an affect on the frequency response of integrator 1904. During the second time period, only third resistor 2306 is shorted out of resistor 2104 by second control signal 2314, which opens second switch 2310. The sum of the resistances of first resistor 2302 and second resistor 2304 affect the frequency response of integrator 1904. During the third time period, none of the three resistors are shorted out of resistor 2104 by the control signals/switches. The sum of the resistances of first resistor 2302, second resistor 2304, and third resistor 2306 affect the frequency response of integrator 1904.

[0208] Note that, although not shown in Table 1, in a fourth time period, first control signal 2312 could be equal to a logical high level, and second control signal 2314 could be equal to a logical low level.

[0209] Also, note that in an actual implementation, the switching action of first and

second switches 2308 and 2310 may cause voltage spikes that appear in integrator output signal 1918. Any such voltage spikes could harm the operation of integrator 1904. Circuit components must be carefully selected and configured to keep the amplitude and duration of any voltage spikes below certain amounts to keep from disturbing the integrator too much.

[0210] In an embodiment, the values for first, second, and third resistors 2302, 2304, and 2306 may be selected such that the value of first resistor 2302 has a lower resistance value than second resistor 2304, and second resistor 2304 has a lower resistance value than third resistor 2306. Other resistor value combinations are also applicable to the present invention.

[0211] FIG. 25A shows frequency responses of integrator 1904 during the three time periods of Table 1, according to an embodiment of the present invention. For the frequency response shown in FIG. 25A, R1 (first resistor 2302) << R2 (second resistor 2304) << R3 (third resistor 2306). FIG. 25A shows a first integrator frequency response 2502 corresponding to the first time period, a second integrator frequency response 2504 corresponding to the second time period, and a third integrator frequency response 2506 corresponding to the third time period.

[0212] FIG. 25B shows a plot of transfer functions for feedback loop 1900 that correspond to first, second, and third integrator frequency responses 2502, 2504, and 2506. FIG. 25B shows a first loop frequency response 2510 that corresponds to third integrator frequency response 2506, a second loop frequency response 2512 that corresponds to second integrator frequency response 2504, and a third loop frequency response 2514 that corresponds to first integrator frequency response 2502. First loop frequency response 2510 has a relatively low high-pass corner frequency of approximately 10 KHz, for example. Second loop frequency response 2512 has a relatively medium high-pass corner frequency of approximately 100 KHz, for example. Third loop frequency response 2514 has a relatively higher high-pass corner frequency of approximately 1 MHz, for example.

[0213] First loop frequency response 2510, second loop frequency response 2512, and third loop frequency response 2514 may be respectively referred to as having a long or slow time constant, a medium time constant, and a short or fast time constant, elsewhere herein. These labels correspond to the RC time constants for their respective configurations of integrator 1904: (R1 + R2 + R3)C for loop frequency response 2510, (R1 + R2)C for loop frequency response 2512, and (R1)C for loop frequency response 2514.

[0214] In an embodiment, one or more feedback loops similar to feedback loop 1900 are present in a receiver channel used to receive WLAN signals. In such an embodiment, different frequency responses for feedback loop 1900 may be used during different portions of the signal receiving process. For example, during the first time period, an initial pass at acquiring DC offset may be made. Accurately acquiring and following DC offset may not be as important during this time period (i.e., a short time constant may be acceptable). During the second time period, an optimal antenna diversity may be searched for and selected. DC offset concerns may become greater during this time period. Also during the first and second time periods, a signal preamble may be received. For example, the preamble may be coded with a Barker word. Hence, DC offset considerations may become more important during this time period (i.e., a medium time constant may be acceptable). During the third time period, a data portion of the data frame corresponding to the received preamble may be received. For example, the data portion may be modulated according to complementary code keying (CCK). The CCK modulated data signal may require the receiver to have a high-pass corner frequency closer to DC than does the Barker coded preamble (i.e., long time constant). Hence, the actions performed during these three time periods may each require a respective receiver frequency response tailored to their special conditions.

[0215] In an embodiment, these three time periods are sequenced through each time a new WLAN signal packet is received. In such an embodiment, for example, the

first time period used to initially acquire DC offset may be within the range of 5 to 6 microseconds. The second time period used to complete the reception of the preamble may be within the range of 55 to 128 microseconds. The third time period may last as long as it is required to receive the entire data portion of the signal packet. In alternative embodiments, one or more of such time periods may be of any duration necessary to support portions of the signal receiving process.

4.3.2 Operation of the Closed Feedback Loop of the Present Invention

[0216] FIG. 27 shows a flowchart 2700 providing operational steps for performing embodiments of the present invention. FIGS. 28, 29, 33, and 34 provide additional operational steps for flowchart 2700, according to embodiments of the present invention. The steps shown in FIGS. 27-29, 33, and 34 do not necessarily have to occur in the order shown, as will be apparent to persons skilled in the relevant art(s) based on the teachings herein. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the following discussion. These steps are described in detail below.

[0217] As shown in FIG. 27, flowchart 2700 begins with step 2702. In step 2702, a first receiver channel signal is received from a first receiver channel node. For example, the first receiver channel signal is output signal 1916, received from output node 1914, as shown in FIG. 19. In an embodiment, the first receiver channel signal is amplified before being received. For example, output signal 1916 may be amplified by first amplifier 1902, which outputs integrator input signal 1920.

[0218] In step 2704, the first receiver channel signal is integrated to generate an integrated signal. For example, integrator input signal 1920 is integrated. For example, integrator input signal 1920 may be integrated by integrator 1904 to generate integrator output signal 1918.

[0219] In step 2706, the integrated signal is summed with a second receiver channel signal at a second receiver channel node. For example, integrator output signal 1918 is summed with receiver channel signal 1912 at summing node 1906. The first receiver channel node is downstream from the second receiver channel node in the receiver channel. As shown in FIG. 19, output node 1914 is further downstream in the receiver channel than is summing node 1906.

[0220] In an embodiment, step 2704 includes the step where the integrated signal is generated as an integrated and inverted version of the first receiver channel signal. For example, integrator 1904 may be configured as an inverting integrator to produce an inverted integrator output signal 1918. In another example, when present, first amplifier 1902 may be configured in an inverting amplifying configuration to produce an inverted integrator input signal 1904, which is input to integrator 1904.

[0221] In an embodiment, step 2704 is performed by an integrator circuit. For example, the integrator circuit is integrator 1904. In an embodiment, the integrator circuit includes an amplifier, a capacitor, and a resistor. For example, integrator 1904 may include amplifier 2102, capacitor 2106, and resistor 2104, as shown in FIG. 21. The present invention is applicable to alternative embodiments for integrator 1904. In an embodiment, flowchart 2700 further includes the step where the amplifier, capacitor, and resistor are arranged in an integrating amplifier configuration. For example, amplifier 2102, capacitor 2106, and resistor 2104, may be arranged in an integrating amplifier configuration as shown in FIG. 21.

[0222] FIG. 28 shows flowchart 2700 with additional optional steps, according to an embodiment of the present invention. In FIG. 28, optional steps are indicated by dotted lines. In an embodiment, flowchart 2700 further includes step 2808. In step 2808, the frequency response of the integrator circuit is varied in response to a control signal. For example, as shown in FIG. 23, integrator 1904 is variable according to first control signal 2312 and second control signal 2314.

[0223] In an embodiment, flowchart 2700 further includes step 2810 shown in FIG.

28. In this embodiment, the integrator includes an amplifier, a capacitor, and a variable resistor. For example, resistor 2104 may be a variable resistor. In step 2810, the value of the variable resistor is varied to alter the frequency response of the integrator. For example, the value of resistor 2104 may be varied to alter the frequency response of integrator 1904.

[0224] In an embodiment, flowchart 2700 further includes step 2812 shown in FIG. 28. In step 2812, the variable resistor is configured. In an embodiment, the variable resistor includes at least one resistor and a switch corresponding to each of the at least one resistor. For example, resistor 2104 includes second resistor 2304 and first switch 2308. In an embodiment, step 2812 includes the step where the corresponding switch is coupled across each of the at least one resistor. For example, first switch 2308 is coupled across second resistor 2304.

[0225] In an embodiment, the variable resistor includes a first resistor, a first switch, a second resistor, a second switch, and a third resistor. For example, resistor 2104 includes first resistor 2302, first switch 2308, second resistor 2304, second switch 2310, and third resistor 2306. In an embodiment, step 2812 includes the following steps, which are shown in FIG. 29:

[0226] In step 2914, the first switch is coupled across the second resistor. For example, first switch 2308 is coupled across second resistor 2304.

[0227] In step 2916, the second resistor is coupled in series with the first resistor. For example, second resistor 2304 is coupled in series with first resistor 2302.

[0228] In step 2918, the second switch is coupled across the third resistor. For example, second switch 2308 is coupled across third resistor 2306.

[0229] In step 2920, the third resistor is coupled in series with the second resistor. For example, third resistor 2306 is coupled in series with second resistor 2304.

[0230] In embodiments, one or more control signals may be supplied to the switches in the variable resistor. The control signals control the opening and closing of the switches, which in turn alters the resistance of the variable resistor. This allows the

frequency response of the integrator to be varied. For example, in an embodiment, step 2812 further includes the following steps, which are shown in FIG. 33:

[0231] In step 3322, a first control signal is received with the first switch. For example, first switch 2308 is received by first control signal 2312.

[0232] In step 3324, a second control signal is received with the second switch. For example, second switch 2310 is received by second control signal 2314.

[0233] In step 3326, the first and second control signals are sequenced according to Table 1, as shown above.

[0234] In an embodiment, step 3326 includes the step where the first and second control signals are sequenced according to the time periods shown in Table 1, where the first time period is in the range of 4 to 6 microseconds, and where the second time period is in the range of 55 to 128 microseconds.

[0235] FIG. 34 shows flowchart 2700 with additional optional steps, according to an embodiment of the present invention. In FIG. 34, optional steps are indicated by dotted lines. In step 3428, a preamble is received during the first and second time periods. For example, a 802.11 WLAN DSSS data frame preamble may be received by a receiver channel incorporating feedback loop 1900, such as receiver channels 1600, 1700, during the first and second time periods. The preamble may be short or long. The receiver may perform diversity switching during these time periods. The present invention is also applicable to receiving additional signal types and formats.

[0236] In step 3430, a data portion of a data frame corresponding to the preamble is received during the third time period. For example, a data portion of the 802.11 WLAN DSSS data frame may be received during the third time period.

[0237] In an embodiment, step 2706 includes the step where the second receiver channel signal is received, where the second receiver channel signal is a radio frequency signal. In an alternative embodiment, step 2706 includes the step where the second receiver channel signal is received, where the second receiver channel signal is an intermediate frequency signal. For example, receiver channel signal 1912

may be a radio frequency or intermediate frequency signal.

[0238] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, in variable frequency response embodiments of the present invention, a plurality of frequency responses for feedback loop 1900 may be sequenced between as necessary to acquire DC offset and receive signal packets of any communication standard type. The invention is intended and adapted to include such alternate embodiments.

4.4 Embodiments for Automatic Gain Control

[0239] Automatic gain control may be used in a communication system receiver channel to maintain the received signal of interest at a useful level. A receiver may use an automatic gain control system to keep the output signal of the receiver at a relatively constant level, despite variations in signal strength at the antenna(s) of the receiver. Automatic gain control makes it possible to range from a weak input signal to a strong input signal without having amplifiers in the receiver channel become saturated. It is important for a receiver to automatically vary the gain of the receiver in such a manner that the receiver will receive a weak signal with high sensitivity but a strong signal with low sensitivity.

[0240] Generally in an automatic gain control system, as described briefly above in section 4.2, a level detector monitors a downstream receiver channel signal. When the downstream receiver channel signal increases or decreases in amplitude, the level detector provides an automatic gain control (AGC) signal to an AGC amplifier upstream in the receiver channel. The AGC signal causes the AGC amplifier to attenuate or amplify the upstream receiver channel signal, accordingly. For example,

FIG. 16 shows example receiver channel 1600 that includes first AGC amplifier 1610 and second AGC amplifier 1604, as described above in section 4.2. First AGC amplifier 1610 receives a first AGC signal 1626 and second AGC amplifier 1604 receives a second AGC signal 1620. First and second AGC signals 1626 and 1620 are generated by corresponding circuitry located downstream from the respective amplifiers. Typically, first and second AGC signals 1626 and 1620 are the same signal, or are generated separately. First AGC amplifier 1610 and second AGC amplifier 1604 amplify their respective receiver channel signals according to first and second AGC signals 1626 and 1620, respectively.

[0241] FIG. 17 shows a receiver channel 1700 with automatic gain control, according to an embodiment of the present invention. Receiver channel 1700 is substantially similar to receiver channel 1600 shown in FIG. 16, except for the configuration of the AGC signals. A first AGC signal 1704 is received by first AGC amplifier 1610. A second AGC signal 1706 is received by second AGC amplifier 1604. Second AGC signal 1706 is equal to first AGC signal 1704, multiplied or amplified by some amount.

[0242] In the embodiment of FIG. 17, multiplier 1702 generates second AGC signal 1706 by multiplying first AGC signal 1704 by a particular amount, shown as N in FIG. 17. This amount may be any value greater than zero (or less than zero if the receiver channel becomes inverted between AGC amplifiers). In a preferred embodiment, this amount is greater than one, and furthermore may be any integer value greater than one.

[0243] FIG. 26 shows an example embodiment for multiplier 1702. Multiplier 1702 as shown in FIG. 26 includes an operational amplifier 2602, a first resistor 2604, and a second resistor 2606 that are arranged in a single-ended non-inverting amplifier configuration. The ratio of first and second resistors 2604 (R1) and 2606 (R2) is selected to provide the gain for multiplier 1702 ($1 + R2/R1$). As a result, multiplier 1702 amplifies first AGC signal 1704 to generate second AGC signal 1706. The

present invention is applicable to other types of signal multipliers, as would be apparent to a person skilled in the relevant art(s) from the teachings herein.

[0244] When the magnitude of N is greater than 1, such as an integer value of 2, second AGC amplifier 1604 reacts more strongly to automatic gain control than does first AGC amplifier 1610, because second AGC signal 1706 has a greater amplitude than does first AGC signal 1704. For example, when second AGC amplifier 1604 is located in a radio frequency (RF) portion of the receiver channel, and the first AGC amplifier 1610 is located in an intermediate frequency (IF) or baseband portion of the receiver channel, the configuration of FIG. 17 allows for a greater reaction at the RF AGC amplifier than at the IF or baseband AGC amplifier. Hence, there is less perturbation in the receiver channel signal at the IF or baseband AGC amplifier. This provides for further advantages in DC offset acquisition and settling time in the receiver channel.

[0245] Furthermore, greater AGC reaction at RF in the receiver channel allows for a greater amplitude signal being received by down-converter 1606 in the receiver channel. Down-converter 1606 is then able to output a greater amplitude down-converted signal 1622. Thus, any DC offsets added into down-converted signal 1622 by down-converter 1606 have less impact proportionally than if down-converted signal 1622 was of lesser amplitude.

[0246] Hence, automatic gain control according to the present invention provides numerous benefits. Additionally, in embodiments, because a single source produces the AGC control signal that is the basis of AGC control for both AGC amplifiers, fewer components are required and less power may be consumed.

[0247] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For example, the present invention

is applicable to AGC implementations in any communication system type, where there are two or more AGC amplifiers. Additional multipliers may be used to produce further AGC signals from the first AGC control signal. The invention is intended and adapted to include such alternate embodiments.

[0248] Examples of the operation of automatic gain control embodiments of the present invention are described in the following sub-section.

4.4.1 Operation of Automatic Gain Control Embodiments of the Present Invention

[0249] FIG. 48 shows a flowchart 4800 providing operational steps for performing embodiments of the present invention. FIGS. 49, 50, and 52 provide additional operational steps for flowchart 4800, according to embodiments of the present invention. The steps shown in FIGS. 48-50 and 52 do not necessarily have to occur in the order shown, as will be apparent to persons skilled in the relevant art(s) based on the teachings herein. Other embodiments will be apparent to persons skilled in the relevant art(s) based on the following discussion. These steps are described in detail below.

[0250] As shown in FIG. 48, flowchart 4800 begins with step 4802. In step 4802, a first AGC signal is multiplied by an amount to generate a second AGC signal. For example, the first AGC signal may be first AGC signal 1704, which is multiplied to generate second AGC signal 1706.

[0251] In step 4804, the first AGC signal is provided to a first automatic gain control (AGC) amplifier coupled in a first portion of the receiver channel. For example, the first AGC amplifier may be first AGC amplifier 1610, as shown in FIG. 17.

[0252] In step 4806, the second AGC signal is provided to a second AGC amplifier coupled in a second portion of the receiver channel. For example, the second AGC amplifier may be second AGC amplifier 1604, which receives second AGC signal

1706.

[0253] FIG. 49 shows flowchart 4800 with additional optional steps, according to an embodiment of the present invention. In FIG. 49, optional steps are indicated by dotted lines. As shown in FIG. 49, flowchart 4800 may further include step 4908. In step 4908, the second AGC amplifier is positioned upstream in the receiver channel from the first AGC amplifier. For example, as shown in FIG. 17, second AGC amplifier 1604 is positioned upstream in the receiver channel from first AGC amplifier 1610.

[0254] FIG. 50 shows flowchart 4800 with additional optional steps, according to an embodiment of the present invention. In FIG. 50, optional steps are indicated by dotted lines. In step 5010, a radio frequency receiver channel signal is received with the second AGC amplifier. For example, input RF signal 1616 may be a radio frequency signal that is received by second AGC amplifier 1604.

[0255] In step 5012, a baseband receiver channel signal is received with the first AGC amplifier. For example, down-converted signal 1622 may be a baseband signal that is received by first AGC amplifier 1610.

[0256] FIG. 52 shows flowchart 4800 with additional optional steps, according to an alternative embodiment of the present invention. In FIG. 52, optional steps are indicated by dotted lines. In step 5214, a radio frequency receiver channel signal is received with the second AGC amplifier. For example, input RF signal 1616 may be a radio frequency signal that is received by second AGC amplifier 1604.

[0257] In step 5216, an intermediate frequency receiver channel signal is received with the first AGC amplifier. For example, down-converted signal 1622 may be an intermediate frequency signal that is received by first AGC amplifier 1610.

[0258] In an embodiment, step 4802 includes the step where the first AGC signal is multiplied by an integer amount to generate the second AGC signal. For example, as shown in FIG. 17, multiplier 1702 may multiply first AGC signal 1704 by an integer amount to generate second AGC signal 1706. In an embodiment, the first

AGC signal is multiplied by 2 to generate the second AGC signal. For example, factor N may be equal to 2.

[0259] In an embodiment, step 4802 includes the step where the first AGC signal is amplified to generate the second AGC signal. For example, first AGC signal 1704 may be amplified by an amplifier such as shown in FIG. 23, to generate second AGC signal 1706.

[0260] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

4.5 Exemplary Receiver Channel Embodiments of the Present Invention

[0261] This section provides further details about various communications system configurations in which embodiments of the present invention may be implemented, and provides further details for implementing these embodiments. These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0262] For exemplary purposes, this section describes the present invention in the context of WLAN communications system configurations. However, the invention is applicable to additional communication system environments. For instance, the invention as disclosed herein is applicable to any type of communication system

receiver. These include wireless personal area network (WPAN) receivers (including the Bluetooth standard), wireless metropolitan area network (WMAN) receivers, code division multiple access (CDMA) receivers including wideband CDMA receivers, Global System for Mobile Communications (GSM) standard compatible receivers, and 3rd Generation (3G) network receivers.

[0263] In actual implementations, one or more embodiments of the present invention may be located in a WLAN receiver channel, such as either of receiver channels 1600 and 1700. The receiver channels may be configured to receive packets formatted according to any WLAN 802.11 standard format, such as direct sequence spread spectrum (DSSS) (including high rate DSSS) and frequency hopping spread spectrum (FHSS). The data rates for these formats include 1, 2, 5.5, and 11 Mbps. Another possible format, orthogonal frequency division multiplexing (OFDM), includes data rates ranging from 6 Mbps to 54 Mbps. Received WLAN signals may have carrier frequencies of 2.4 and 5.0 GHz, and others. The modulation techniques used for these various formats include phase shift keying (PSK), differential binary phase shift keying (DBPSK), differential quadrature phase shift keying (DQPSK), Gaussian frequency shift keying (GFSK), 16- and 64-quadrature amplitude modulation (QAM), packet binary convolutional coding (PBCC) modulation, and complementary code keying (CCK) modulation.

[0264] Receiver channels according to the present invention may have a variety of configurations. The embodiments of the present invention described above are adaptable to being implemented in either single-ended or differential receiver channels. It is noted that even-order inter-mod products may be more effectively canceled in differential implementations. Hence, in some applications, differential implementations may be desirable.

[0265] FIGS. 31A and 31B show further details of receiver channel 1700, according to an exemplary embodiment of the present invention. FIGS. 31A and 31B also incorporate examples of feedback loop 1900 and automatic gain control, according

to embodiments of the present invention. FIG. 31A shows a first portion of receiver channel 1700, including an antenna 1614, optional low noise amplifier 1602, second AGC amplifier 1604, down-converter 1606, and first amplifier/filter section 1608. FIG. 31B shows a second portion of receiver channel 1700, including first AGC amplifier 1610, second optional amplifier/filter section 1612, and multiplier 1702.

[0266] As shown in FIG. 31A, down-converter 1606 may be a UFD module. The UFD module receives a control signal 3106. Alternative types of down-converters may be used for down-converter 1606, according to embodiments of the present invention.

[0267] Amplifier-filter section 1608 is shown including a first amplifier 3110, a filter 3112, and a feedback loop 1900a. First amplifier 3110 provides for gain in amplifier-filter section 1608. Filter 3112 provides for filtering in amplifier-filter section 1608. Feedback loop 1900a provides for gain and for DC offset voltage reduction in amplifier-filter section 1608. Feedback loop 1900a includes a first amplifier 1902a, a second amplifier 1908a, and an integrator 1904a. The elements of feedback loop 1900a operate as described for the similarly designated elements of feedback loop 1900 shown in FIG. 19. Feedback loop 1900a measures a DC offset voltage at output node 1914a, and subtracts the measured DC offset voltage from the receiver channel at summing node 1906a.

[0268] Integrator 1904a provides for a variable frequency response, similarly to that of integrator 1904 shown in FIG. 23. Integrator 1904a receives two control signals, ACQ1 3104 and ACQ2 3102, that control the opening and closing of switches 2308a and 2310a in integrator 1904a, in order to vary the frequency response of feedback loop 1900a.

[0269] Second amplifier 1908a provides for receiver channel gain between summing node 1906a and output node 1914a. First amplifier 1902a provides for gain in the feedback loop.

[0270] As stated above, receiver channel 1700 shown in FIGS. 31A and 31B include

automatic gain control features of the present invention. The AGC features of the present invention are more fully described in section 4.4. As shown in FIG. 31B, multiplier 1702 receives first AGC signal 1704 and generates second AGC signal 1706. Second AGC signal 1706 is input to second AGC amplifier 1604 in FIG. 31A. First AGC signal 1704 is input to first AGC amplifier 1610 in FIG. 31B. Multiplier 1702 is shown in FIG. 31B as an operational amplifier implemented in a non-inverting configuration, but may be implemented in alternative configurations. The AGC signals for second AGC amplifier 1604 and first AGC amplifier 1610 are based upon a single AGC signal source. Furthermore, multiplier 1702 allows for faster gain control in second AGC amplifier 1604 than in first AGC amplifier 1610, by amplifying first AGC signal 1704 to generate a greater amplitude second AGC signal 1706.

[0271] Amplifier-filter section 1612 is shown to include feedback loop 1900b in FIG. 31B. Feedback loop 1900b provides for gain and for DC offset voltage reduction in amplifier-filter section 1612. Feedback loop 1900b includes a first amplifier 1902b, a second amplifier 1908b, and an integrator 1904b. The elements of feedback loop 1900b operate as described for the similarly designated elements of feedback loop 1900 shown in FIG. 19. Feedback loop 1900b measures a DC offset voltage at output node 1914b, and subtracts the measured DC offset voltage from the receiver channel at summing node 1906b.

[0272] Integrator 1904b provides for a variable frequency response, similarly to that of integrator 1904 shown in FIG. 23. Integrator 1904b receives the two control signals ACQ1 3104 and ACQ2 3102, that control the opening and closing of switches 2308b and 2310b (and of switches 2308a and 2310a in integrator 1904a shown in FIG. 31A) in integrator 1904b of FIG. 31B, in order to vary the frequency response of feedback loop 1900b.

[0273] Second amplifier 1908b provides for receiver channel gain between summing node 1906b and output node 1914b. First amplifier 1902b provides for gain in the

feedback loop.

[0274] The present invention is applicable to any 802.11 WLAN receiver implementations, including differential receiver channel configurations. FIGS. 32A and 32B show further details of receiver channel 1700, according to an example differential receiver channel embodiment of the present invention. FIGS. 32A and 32B incorporate embodiments of feedback loop 1900 and automatic gain control, according to embodiments of the present invention. FIG. 32A shows a first portion of receiver channel 1700, including second AGC amplifier 1604, first amplifier/filter section 1608, and multiplier 1702. FIG. 32B shows a second portion of receiver channel 1700, including first AGC amplifier 1610 and second optional amplifier/filter section 1612. An antenna and down-converter are not shown in the portions of receiver channel 1700 shown in FIGS. 32A and 32B. FIG. 30 shows a differential UFD module that may be used as a differential down-converter in down-converter 1606 shown in FIGS. 16 and 17, according to embodiments of the present invention. The invention is also applicable to other types of differential down-converters.

Sub a8

[0275] As shown in FIG. 32A, an input differential signal 3210 is received by second AGC amplifier 1604. Input differential signal 3210 is a differential signal, and second AGC amplifier 1604 is a differential AGC amplifier. Input differential signal 3210 may be a differential version of a received RF signal or IF signal, for example.

Sub a9

[0276] Amplifier-filter section 1608 is shown as a first amplifier 3202, a second amplifier 3204, a first filter 3206, a second filter 3208, and feedback loop 1900c. First and second amplifiers 3202 and 3204 receive the differential output of second AGC amplifier 1604, and provide gain to the + and - components of this signal. First and second filters 3206 and 3208 provide for filtering of the + and - components of the differential output of second AGC amplifier 1604.

[0277] Feedback loop 1900c provides for gain and for DC offset voltage reduction for the differential signal output by first and second filters 3206 and 3208. Feedback

loop 1900c includes a first amplifier 1902c, a second amplifier 1908c, and an integrator 1904c. The elements of feedback loop 1900c operate as described for the similarly designated elements of feedback loop 1900 shown in FIG. 19. Feedback loop 1900c receives the amplified and filtered differential signal output of second AGC amplifier 1604 at summing node 1906c. Feedback loop 1900c measures a DC offset voltage at output node 1914c, and subtracts the measured DC offset voltage from the receiver channel at summing node 1906c.

[0278] Second amplifier 1908c provides for receiver channel gain between summing node 1906c and output node 1914c. Second amplifier 1908c includes two amplifiers configured differentially in series.

[0279] First amplifier 1902c provides for gain in the feedback loop. First amplifier 1902c receives a receiver channel differential signal 3212 that is output from second amplifier 1908c, and outputs a single-ended output signal 1920.

[0280] Integrator 1904c provides for a variable frequency response, similarly to that of integrator 1904 shown in FIG. 23. Integrator 1904c receives single-ended output signal 1920. Integrator 1904c also receives two control signals, ACQ1 3104 and ACQ2 3102, that control the opening and closing of switches 2308c and 2310c in integrator 1904c, in order to vary the frequency response of feedback loop 1900c.

Sub a4

[0281] As stated above, receiver channel 1700 shown in FIGS. 32A and 32B include automatic gain control features of the present invention. These features are more fully described in section 4.4. As shown in FIG. 32A, multiplier 1702 receives first AGC signal 1704 and generates second AGC signal 1706. Second AGC signal 1706 is input to second AGC amplifier 1604 in FIG. 32A. First AGC signal 1704 is input to first AGC amplifier 1610 in FIG. 32B. Multiplier 1702 is shown in FIG. 32A as an operational amplifier implemented in a non-inverting configuration, but may be implemented in alternative configurations. The AGC signals for second AGC amplifier 1604 and first AGC amplifier 1610 are based upon a single AGC signal source that generates first AGC signal 1704. Furthermore, multiplier 1702 allows for

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faster gain control in second AGC amplifier 1604 than in first AGC amplifier 1610, by amplifying first AGC signal 1704 to generate a greater amplitude second AGC signal 1706.

Sub a5

[0282] In FIG. 32B, first AGC amplifier 1610 receives receiver channel differential signal 3212, and outputs an amplified differential signal.

[0283] Amplifier-filter section 1612 includes feedback loop 1900d. Feedback loop 1900d provides for gain and for DC offset voltage reduction in amplifier-filter section 1612. Feedback loop 1900d includes a first amplifier 1902d, a second amplifier 1908d, and an integrator 1904d. The elements of feedback loop 1900d operate as described for the similarly designated elements of feedback loop 1900 shown in FIG. 19. Feedback loop 1900d receives the amplified differential signal output of first AGC amplifier 1610 at summing node 1906d. Feedback loop 1900d measures a DC offset voltage at output node 1914d, and subtracts the measured DC offset voltage from the receiver channel at summing node 1906d.

[0284] Second amplifier 1908d provides for receiver channel gain between summing node 1906d and output node 1914d. Second amplifier 1908d includes four amplifiers configured differentially in series, with a single-ended output, output signal 1628.

Sub a6

[0285] First amplifier 1902d provides for gain/attenuation in the feedback loop. First amplifier 1902d is shown in FIG. 32B as a resistor voltage-divider circuit. First amplifier 1902d receives and attenuates output signal 1628 according to the voltage divider, and outputs an attenuated output signal 1920d.

Sub a7

[0286] Integrator 1904d provides for a variable frequency response, similarly to that of integrator 1904 shown in FIG. 23. Integrator 1904d receives the two control signals ACQ1 3104 and ACQ2 3102, that control the opening and closing of switches 2308d and 2310d (and switches 2308c and 2310c in integrator 1904c shown in FIG. 32A) in integrator 1904d of FIG. 32B, in order to vary the frequency response of feedback loop 1900d.

[0287] FIGS. 35-37 show exemplary frequency response waveforms for receiver

channel 1700 configured as shown in FIGS. 31A-B and 32A-B, when the frequency response is varied. The frequency responses shown in FIGS. 35-37 for receiver channel 1700 may be varied as needed by the particular application, by selecting the circuit components accordingly. As stated above, a down-converter is not present in the portion of the receiver channel shown in FIGS. 32A-B, so frequency down-conversion does not occur in the portion of receiver channel 1700 shown in FIGS. 32A-B.

Sub a8

[0288] FIG. 35 shows a first frequency response waveform 3500 resulting when ACQ1 3104 and ACQ2 3102 are both set to high. This setting indicates a short time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-B. As can be seen in FIG. 35, a high-pass corner frequency for first frequency response waveform 3500 is located near 2.5 MHz.

Sub a9

[0289] FIG. 36 shows a second frequency response waveform 3600 resulting when ACQ1 3104 is set to a high level and ACQ2 3102 is set to a low level. This setting indicates a medium time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-B. As can be seen in FIG. 36, a high-pass corner frequency for second frequency response waveform 3600 is located near 269 KHz.

Sub a10

[0290] FIG. 37 shows a third frequency response waveform 3700 resulting when ACQ1 3104 and ACQ2 3102 are both set to low levels. This setting indicates a long time constant has been selected for integrators 1904a and 1904b in FIGS. 31A-B, or for integrators 1904c and 1904d in FIGS. 32A-B. As can be seen in FIG. 37, a high-pass corner frequency for third frequency response waveform 3700 is located near 21.6 KHz.

[0291] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the

embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

4.5.1 Using the Receiver Channel of the Present Invention to Receive a WLAN Signal Packet

[0292] The section provides examples of how embodiments of the present invention may be used to receive signal frames or packets, and in particular, to receive WLAN signal packets. WLAN signal frames are briefly described. Selection of antenna diversity is described, and the use of variable frequency response according to the present invention is described in relation to receiving a WLAN signal frame. These embodiments are described herein for purposes of illustration, and not limitation. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

[0293] As mentioned above, receiver channels 1600 and 1700 may be used to receive WLAN signals. For example, as described as follows, receiver channel 1700 may receive a transmitted WLAN DSSS frame modulated according to DQPSK, and having a short preamble. The short preamble portion of the frame is received first, and includes a 56 bit SYNC field that a receiver uses to acquire the subsequent portions of the signal. In this example, the preamble data rate is 1 Mbps. After receiving the preamble, a portion of the frame called a SFD follows. The SFD field contains information marking the start of the PSDU frame. The PSDU is the data field for the DSSS frame.

[0294] FIG. 39 shows an example timeline 3900 for receiving a DSSS frame.

Timeline 3900 includes a first time segment 3902, a second time segment 3904, a third time segment 3906, a fourth time segment 3908, a fifth time segment 3910, a sixth time segment 3912, and a seventh time segment 3914. In the example of FIG. 39, the receiver includes two switchable antennas (i.e., dual diversity). During time segments shown in FIG. 39, the receiver switches between the two antennas, labeled antennas A and B, to determine which antenna is best suited to receive the remainder of the frame. In FIG. 39 each of the time segments, except for first time segment 3902, last for 10 μs. In alternative embodiments, there may be more or fewer time segments, and they may last for longer or shorter segments of time. For example, if the preamble was a long preamble (128 bits), there may be the same number of time segments, but they could each last for 20 μs instead of 10 μs. Alternatively, there could be a larger number of time segments.

[0295] As shown in FIG. 39, during first time segment 3902, which lasts 2 μs, the transmitted signal ramps up. During first time segment 3902 and second time segment 3904, which lasts 10 μs, the first antenna, antenna A, is selected to receive the transmitted signal. During third time segment 3906, which lasts 10 μs, the second antenna, antenna B, is selected to receive the transmitted signal. During fourth time segment 3908, which lasts 10 μs, antenna A, is again selected to receive the transmitted signal. During fifth time segment 3910, which lasts 10 μs, antenna B is again selected to receive the transmitted signal. During sixth time segment 3912, which lasts 14 μs, the one of antennas A and B, that was chosen to receive the transmitted signal is selected to receive the transmitted signal frame. During seventh time period 3914, the SFD frame portion and remainder of the DSSS frame are received using the chosen antenna.

[0296] FIG. 38 shows example waveforms related to the operation of receiver channel 1700 as shown in FIGS. 32A-B in a WLAN environment, according to an embodiment of the present invention. The waveforms of FIG. 38 relate to receiving the preamble of the above described DSSS frame. The waveforms shown in FIG. 38

are output signal 1628, second AGC signal 1706, integrator output signal1918c, and AGC2 3102. FIG. 38 shows integrator output signal 1918c, which is related to feedback loop 1900c, but it is understood to persons skilled in the relevant art(s) from the teachings herein that integrator output signal 1918d is similar, even though not shown.

Sub a11

[0297] Receiver channel 1700 as shown in FIGS. 32A and 32B provides for gain, filtering, and DC offset voltage reduction for input differential signal 3210. Output signal 1628, shown in FIG. 32B, is the output signal for receiver channel 1700. As can be seen in the embodiment of FIG. 38, output signal 1628 is an approximately 1 MHz information signal.

[0298] ACQ2 3102 is shown as a logical high from 0 to about 4 μs (FIG. 38 shows ACQ2 3102 transitioning to a logic low at about 4 μs). During this period, ACQ1 3104 is also high (not shown), so feedback loops 1900c and 1900d are causing receiver channel 1700 to operate with a frequency response similar to first frequency response 3500 shown in FIG. 35 (i.e., fast time constant). First frequency response 3500 shows low gain as DC is approached, so DC offset acquisition by feedback loops 1900c and 1900d is not as significant during this time period. For example, integrator output signal 1918c in FIG. 38, shows the amount of DC offset being fed back to be subtracted from the receiver channel signal at summing node 1906c. This time period coincides roughly with first time segment 3902 and a portion of second time segment 3904 shown in FIG. 39.

[0299] ACQ2 3102 transitions to a logical low level at around 4 μs, as shown in FIG. 38. ACQ1 3104 remains high (not shown), so feedback loops 1900c and 1900d are causing receiver channel 1700 to operate with a frequency response similar to second frequency response 3600 shown in FIG. 36 (i.e., medium time constant). Receiver channel 1700 retains this frequency response for most of the remainder of the timeline 3900. Second frequency response 3600 shows moderate gain as DC is approached, so DC offset acquisition by feedback loops 1900c and 1900d is more

significant during this time period. Integrator output signal 1918c shown in FIG. 38, operates with improved DC offset accuracy during this time period, due to the medium time constant selection.

[0300] While ACQ2 3102 and ACQ1 3104 remain in this state, receiver channel 1700 begins to switch between antennas A and B to determine which is best suited to receive the incoming DSSS frame. During the time period of approximately 4 μs through 14 μs, corresponding to second time segment 3904 shown in FIG. 39, antenna A is selected. During this time period, second AGC signal 1706 ramps up to increase the gain of first AGC amplifier 1908c. This increase in gain is reflected in output signal 1628, which increases in amplitude. Second AGC signal 1706 is increased because downstream processing determined that the amplitude of output signal 1628 was initially too low, with antenna A as the input antenna.

[0301] The amount of DC offset detected also increases during this time period, due to the increase in gain, as reflected in integrator output signal 1918c. During the time period from about 4 μs to about 12 μs, it can be seen that the absolute offset of output signal 1628 from zero volts, which initially is significant (the center of output signal 1628 is at about -0.2 V at 4 μs), is reduced to be essentially equal to zero volts. This decrease is caused by an increase in integrator output signal 1918c during this time period, which feeds back the DC offset to be summed with the receiver channel.

[0302] During the time period of approximately 14 μs through 24 μs, corresponding to third time period 3906 shown in FIG. 39, antenna B is selected. During this time period, second AGC signal 1706 is decreased to decrease the gain of first AGC amplifier 1908c. This decrease in gain is reflected in output signal 1628, which initially increases sharply with the switch to antenna B, and then decreases in amplitude. Second AGC signal 1706 is decreased because downstream processing determined that the amplitude of output signal 1628 was initially too high, with antenna B as the input antenna.

[0303] The amount of DC offset detected also decreases during this time period, due

to the decrease in gain, as reflected in integrator output signal 1918c. During the time period from about 14 μs to about 18 μs, it can be seen that the absolute offset of output signal 1628 initially increases, and then is decreased. The offset of output signal 1628 was initially significant (the center of output signal 1628 is at about 0.5 V at 16 μs), is reduced to be essentially equal to zero volts. This decrease is caused by an decrease in integrator output signal 1918c during this time period, which feeds back the DC offset to be summed with the receiver channel.

[0304] The process of switching between antenna A and antenna B continues during the next two time periods of 24 μs to 34 μs, and 34 μs to 44 μs. These correspond to fourth and fifth time segments 3908 and 3910 shown in FIG. 39. Similar results are found during these two time periods as occurred during the previous two.

[0305] As shown in the following time period, 44 μs to 54 μs, which corresponds to sixth time segment 3912, antenna B is selected to receive the DSSS frame. At the beginning of the next time period, corresponding to seventh time segment 3914 shown in FIG. 39, ACQ2 3104 will transition to a logical low level while ACQ1 3104 remains low (not shown in FIG. 38). In this state, feedback loops 1900c and 1900d will cause receiver channel 1700 to operate with a frequency response similar to third frequency response 3700 shown in FIG. 37 (i.e., slow time constant). Receiver channel 1700 retains this frequency response for the remainder of the DSSS frame. Third frequency response 3700 shows relatively greater gain as DC is approached, so DC offset acquisition by feedback loops 1900c and 1900d is even more significant during this time period. In other words, feedback loops 1900c and 1900d will track the DC offset with greater accuracy, due to the slow time constant selection.

[0306] It should be understood that the above examples are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant

art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

4.5.2 Embodiments for Generating Control Signals for a Receiver Channel According to the Present Invention

[0307] This section provides embodiments for generating control signals used to vary the frequency response of a receiver channel, according to embodiments of the present invention. For example, this section relates to circuits and modules used to generate first and second control signals 2312 and 2314 shown in FIG. 23 and generating ACQ1 3104 and ACQ2 3102 shown in FIGS. 31A-32B. Varying the frequency response of a receiver channel may be used to enhance DC offset reduction, as described above. A window comparator for monitoring the level of DC offset is described. A state machine for sequencing the control signals is also described. The state machine may receive the output of the window comparator as an input, among other input signals.

4.5.2.1 Window Comparator for Monitoring DC Offset

[0308] A window comparator according to the present invention may be used to monitor a signal in a receiver channel, and determine whether the level of DC offset in the receiver channel is within an acceptable range. FIG. 41 shows a high level view of a window comparator module 4100, according to an embodiment of the present invention. The implementations for window comparator module 4100 below are described herein for illustrative purposes, and are not limiting. In particular, window comparator module 4100 as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software,

or any combination thereof.

[0309] Window comparator module 4100 receives an I channel input signal 4102 and a Q channel input signal 4104. For example, I channel input signal 4102 and Q channel input signal 4104 may be output signals of respective receiver channels, such as output signal 1628 shown in FIGS. 16 and 17, or may be upstream signals in the respective receiver channels. Window comparator module 4100 determines whether a DC offset in each of I channel input signal 4102 and Q channel input signal 4104 is within an acceptable range. Window comparator module 4100 outputs window compare (WC) signal 4106, which indicates whether both of I channel input signal 4102 and Q channel input signal 4104 are within acceptable ranges.

[0310] Window comparator module 4100 as shown in FIG. 41 accepts as input I and Q channel signals, but in alternative embodiments may accept a single channel signal as input, or may accept additional input channel signals.

[0311] FIG. 42 shows further detail of an exemplary window comparator module 4100, according to an embodiment of the present invention. Window comparator module 4100 includes a prefilter 4202, a window comparator 4204, a filter 4208, a magnitude comparator 4212, and an AND gate 4216. FIG. 42 shows the components of a window comparator module 4100 used to provide the window compare function for I channel input signal 4102. AND gate 4216 is optional, and may be present when more than one receiver channel signal is input to window comparator module 4100, as in the embodiment shown in FIG. 41.

[0312] Prefilter 4202 receives and filters I channel input signal 4102, and outputs a filtered signal 4220. Prefilter 4202 is optional, and is present when I channel input signal 4102 requires filtering. For example, prefilter 4202 may be used to remove data/symbol variance. Prefilter 4202 may be any suitable filter type.

[0313] Window comparator 4204 receives filtered signal 4220 and voltage reference 4206. Window comparator 4204 compares the voltage level of filtered signal 4220 to determine whether it is within a voltage range centered upon the voltage value of

voltage reference 4206. For example, voltage reference 4206 may be zero when zero is the reference value for the receiver channel, or may be another value such as 1.5 volts, or any other reference voltage value. In one example, the voltage range may be +/- 50 mV around the value of voltage reference 4206. Window comparator 4204, for example, may include two analog comparators. The first analog comparator may determine whether filtered signal 4220 is above a maximum value of the voltage range, and the second analog comparator may determine whether filtered signal 4220 is below a minimum value of the voltage range. Preferably, window comparator outputs a logical output signal, compare value 4222. For example, compare value 4222 may be a logical high value when the voltage level of filtered signal 4220 is within the voltage range, and a logical low level when the voltage level of filtered signal 4220 is outside the voltage range.

[0314] Filter 4208 receives compare value 4222 and clock 4210. Filter 4208 outputs a value providing an indication of how well I channel input signal 4102 is remaining within the voltage range. For example, filter 4208 may provide an output that indicates how many clock cycles of clock 4210 that filter signal 4220 was found to be within the voltage range, during some number of the last clock cycles. In embodiments, filter 4208 may be a finite impulse response (FIR) or an infinite impulse response (IIR) filter. Preferably, filter 4208 outputs a logical output value, filter output 4222, that provides the indication.

[0315] FIG. 43 shows an example embodiment for window comparator module 4100, where filter 4208 includes a FIR filter. The FIR filter of filter 4208 includes a plurality of registers 4302a through 4302k (12 registers in this example) that store and shift values of compare value 4222 during each cycle of clock 4210. In the embodiment of FIG. 43, clock 4210 is shown to be an 11 MHz clock, but may instead be of alternative clock cycles rates. Registers 4302a through 4302k provide register output signals 4304a through 4304k, which are the shifted and stored values of compare value 4222. In embodiments, register output signals 4304a through 4304k

may be weighted (not shown). Register output signals 4304a through 4304k are summed by summer 4306. Summer 4306 outputs a summed signal 4224, which is essentially a sum of the previous k values of compare value 4222.

[0316] As shown in FIG. 43, filter 4208 may receive a WC reset signal 4308 that is used to reset registers 4302a through 4302k to a low logical output value. WC reset signal 4308 may be used at power up, and at other times during the operation of a receiver channel, when it is desired to re-start the monitoring of a receiver channel signal for DC offset.

[0317] As shown in FIGS. 42 and 43, magnitude comparator 4212 receives summed signal 4224 and a threshold value 4214. Magnitude comparator 4212 compares the value of summed signal 4224 to threshold value 4214. If summed signal 4224 is greater than threshold value 4214, magnitude comparator 4212 outputs a logical high value on a I channel WC signal 4226, indicating that a DC offset voltage level in I channel input signal 4102 has been determined to be within an acceptable voltage range for enough of the designated length of time. If summed signal 4224 is less than or equal to threshold value 4214, I channel WC signal 4226 is a logical low value, indicating that a DC offset voltage level in I channel input signal 4102 has been determined to be outside of an acceptable voltage range for too much of the designated length of time. In the example of FIG. 43, threshold 4214 is shown in be equal to 7 (out of 12 cycles), but may be equal to other values.

[0318] When AND 4216 is present, AND 4216 receives I channel WC signal 4226 and comparable signal for every other channel being monitored by window comparator module 4100. AND 4216 outputs WC signal 4106 that indicates whether all receiver channels have acceptable DC offset values. FIG. 42 shows AND 4216 receiving I channel WC signal 4226 for the I channel, and Q channel WC signal 4218 for the Q channel. When both of I and Q channel WC signals 4226 and 4218 are equal to a high logical value, indicating that both channels are within the acceptable DC offset voltage range, AND 4216 outputs a logical high value on WC signal 4106.

When either or both of I and Q channel WC signals 4226 and 4218 are not equal to a logical high value, WC signal 4106 is a logical low value.

[0319] FIG. 44 shows example waveforms related to the operation of window comparator 4100, according to an embodiment of the present invention. FIG. 44 shows waveforms for I channel input signal 4102, filtered signal 4220, and I channel WC signal 4226 of FIG. 43.

[0320] I channel input signal 4102 is an I channel receiver signal to be monitored, which is shown as a data signal that is triangle modulated with DC offset. Filtered signal 4220 is a filtered version of I channel input signal 4102, where the higher frequency oscillating data information is filtered out, and the lower frequency DC offset voltage remains. For the example of FIG. 44, reference voltage 4206 is equal to 1.65 V, and the desired DC offset voltage range is 1.6 V to 1.7 V (+/- .05V around 1.65V).

[0321] As shown in I channel WC signal 4226, as filtered signal 4220 moves above 1.7 V, and moves below 1.6 V, for a long enough period of time, I channel WC signal 4226 is a logical low level, indicating an unacceptable amount of DC offset. As long as I channel WC signal 4226 remains between 1.6 V and 1.7 V, I channel WC signal 4226 is a logical high signal, indicating an acceptable amount of DC offset.

[0322] It should be understood that the above examples for window comparator module 4100 are provided for illustrative purposes only. The invention is not limited to this embodiment. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. The invention is intended and adapted to include such alternate embodiments.

4.5.2.2 State Machine for Generating Control Signals

[0323] FIG. 45 shows an example state machine module 4500 for generating and sequencing control signals of the present invention, such as first and second control signals 2312 and 2314 shown in FIG. 23, and ACQ1 3104 and ACQ2 3102 shown in FIGS. 31A-32B. Implementations for state machine 4500 are described herein for illustrative purposes, and are not limiting. In particular, state machine 4500 as described in this section can be achieved using any number of structural implementations, including hardware, firmware, software, or any combination thereof.

[0324] State machine module 4500 according to the present invention may receive one or more of a variety of inputs that are used to generate control signals. FIG. 45 shows an embodiment of state machine module 4500 that receives WC signal 4106, a PCM signal 4502, a diversity signal 4504, and a clock signal 4506. State machine 4500 generates ACQ1 3104 and ACQ2 3102. In alternative embodiments, state machine module 4500 may receive fewer or more inputs, and may generate fewer or more outputs than shown in FIG. 45.

[0325] In an embodiment, PCM signal 4502 provides one or more bits of data to state machine module 4500 that indicate the mode or state of the communication system that includes the receiver channel. Hence, PCM signal 4502 provides information that indicates whether state machine module 4500 needs to be operating, for example. For instance, in an embodiment, PCM signal 4502 provides a two bit-wide signal to state machine module 4500, in the form of bits PCM1 and PCM2. The communication system modes provided to state machine module 4500 via PCM1 and PCM2 are shown in the table below:

Mode	PCM1	PCM2
Off	0	0
Standby	0	1
Transmitting	1	0
Receiving	1	1

Table 2

"Off" mode is where the communication system that includes the receiver channel is not operating. "Standby" mode is where the communication system is in a standby or wait state. "Transmitting" mode is where the communication system is currently in a transmitting state. "Receiving" mode is where the communication system is in a receiving state. In an embodiment, state machine module 4500 only needs to be active when the communication system is in receiving mode. Hence, in such an embodiment, state machine module 4500 will only be active when PCM1 and PCM2 are both equal to a logical high level, as shown in the above table.

[0326] In an embodiment, state machine module 4500 receives WC signal 4106, as further described in section 4.5.2.1 above. As described above, WC signal 4106 provides an indication of whether the level of DC offset in the receiver channel is within an acceptable range. WC signal 4106 is a logical high level when DC offset is within an acceptable range, and is a logical low level when DC offset is outside of the acceptable range. Hence, when state machine module 4500 receives a logical low or high level on WC signal 4106, state machine may manipulate ACQ1 3104 and ACQ2 3102 to cause the receiver channel to change the DC offset acquisition mode, as described above in section 4.3.1 in regards to first and section control signals 2312 and 2314.

[0327] For example, DC offset in receiver channel 1600 or 1700 may be drifting out of the acceptable voltage range, when the receiver channel is operating according to a slow time constant. When the receiver channel is operating according to a slow

time constant, ACQ1 3104 and ACQ2 3102 are set to logical low levels. Hence, the receiver channel will have a frequency response with a relatively lower 3 dB cutoff frequency, and a relatively larger amount of 1/f noise, as shown in FIG. 40, may be passing through the receiver channel. This larger amount of 1/f noise may contribute to the DC offset drifting out of the acceptable range. Hence, when WC signal 4106 transitions to a low logical level, indicating that DC offset is out of an acceptable range, one or both of ACQ 3104 and ACQ2 3102 may be set to logical high levels in order to select a medium or faster time constant, to select a frequency response for the receiver channel with a relatively higher high-pass corner frequency. These time constants will cause the receiver channel to filter out more of the 1/f noise, and possibly allow the receiver channel to better attain and remove the DC offset, to bring the receiver channel DC offset back into an acceptable DC offset voltage range.

[0328] Furthermore, although not shown in FIG. 45, state machine module 4500 may output WC reset signal 4308, shown as an input signal to waveform comparator 4100 in FIG. 43. In FIG. 43, WC reset signal 4308 is used to reset filter 4208, which has been keeping track of how long the DC offset has been out of range. State machine module 4500 may toggle WC reset signal 4308 for various reasons, including at power up and during a transition from transmitting to receiving modes.

[0329] Diversity signal 4505 is a one or more bit wide signal that at least provides an indication of antenna diversity transitions. For example, a first bit of diversity signal 4505, b[0], may transition from a logic low to a logic high, and vice versa, when a transition from one diversity antenna to another occurs. Diversity signal 4505 may provide further bits of information that indicate the type of diversity antenna search being performed.

[0330] Clock signal 4506 is received to control the timing for state machine module 4500. Clock signal 4506 may be the same as or different from clock 4210.

[0331] FIG. 46 shows a state diagram 4600, according to an exemplary embodiment of the present invention. State diagram 4600 may be implemented in state machine

module 4500 to generate signals ACQ1 3104, ACQ2 3102, and WC reset signal 4308. State diagram 4600 includes states 4602, 4604, 4606, 4608, 4610, and 4612. State diagram 4600 is particularly applicable to a WLAN environment, and is applicable to both short preamble (e.g., 56 μS) and long preamble (e.g., 128 μS) data frames, for example. Time periods are provided below for the length of time that some of the states are active. In a WLAN environment, the time periods, and corresponding levels of ACQ1 3104 and ACQ2 3102, correspond to the time periods shown in FIG. 39 above.

[0332] In the embodiment of state diagram 4600, clock signal 4506 is used to control timing. PCM 4502 is a two bit-wide input signal formed from PCM1, PCM2, as further described above. ACQ1 3104 and ACQ2 3102 form a two-bit wide signal named ACQ in state diagram 4600, in the bit order of ACQ1 3104, ACQ2 3102. A signal TOUT is shown in state diagram 4600. When TOUT is shown equal to zero during a transition from a first state to a second state, this indicates that a time period defined by the first state has expired. In the embodiment of state diagram 4600, WC reset signal 4308 may or may not be generated, although it is shown as generated in state diagram 4600.

[0333] Diversity signal 4504 provides an antenna diversity transition indication to state diagram 4600, through b[0], as described above. A logical high or low level of signal b[0] each indicate a respective diversity antenna setting. A signal B[0] is used to represent an updated version of b[0]. The signals b[0] and B[0] are compared to detect a diversity antenna transition. When b[0] is not equal to B[0], a diversity antenna transition has just occurred. When they are equal, a diversity transition has not occurred. When a diversity antenna has finally been selected for the WLAN data frame, b[0] will become dormant.

[0334] The states of state diagram 4600 are further described as follows.

[0335] State 4602 shown in FIG. 4600 is the active state upon power-up/reset. After system power up, the active state transitions from state 4602 to state 4604 via a

transition 4614. PCM is set to 00, which signifies an "off" mode for state machine module 4500. Also, at system power up, B[0] equals b[0].

[0336] When active, state 4604 is an off state for state machine module 4500. State 4606 is remained in when the communication system remains in a mode other than a receiving mode, such as "off", "standby", or "transmitting." As long as PCM does not change to 11 (receiving mode), a transition 4616 transitions from state 4604 back to state 4604. When PCM transitions to be equal to 11, (receiving mode), the active state transitions from state 4604 to state 4606 via a transition 4618.

[0337] In state 4606, ACQ is equal to 11. In other words, ACQ1 3104 and ACQ2 3102 are selecting a short time constant for DC offset acquisition. Furthermore, WC reset signal 4308 may be set equal to 1 for a clock cycle during the transition to state 4606, to reset the DC offset acquisition registers of window comparator module 4100. In an embodiment, state 4606 is active for a first time period of 6 μS. After the first time period in state 4606 expires, the active state transitions from state 4606 to state 4608 via a transition 4620.

[0338] In state 4608, ACQ is equal to 10. In other words, ACQ1 3104 and ACQ2 3102 are selecting a medium time constant for DC offset acquisition. In an embodiment, state 4608 is active for a second time period of 12 μS. If a diversity transition occurs while state 4608 is active, (i.e., B[0] is not equal to b[0]) a transition 4622 transitions from state 4608 back to state 4608. State 4608 is thus again active for a new second time period of 12 μS. However, after second time period in state 4608 expires, the active state transitions from state 4608 to state 4610 via a transition 4624.

[0339] In state 4610, ACQ is equal to 10. In other words, ACQ1 3104 and ACQ2 3102 are continuing to select a medium time constant for DC offset acquisition. In an embodiment, state 4610 is active for a third time period of 9 μS. If a diversity transition occurs while state 4610 is active (i.e., B[0] is not equal to b[0]), the active state transitions from state 4610 back to state 4608 via a transition 4626. After third

time period in state 4610 expires, the active state transitions from state 4610 to state 4612 via a transition 4628.

[0340] In state 4612, ACQ is equal to 00. In other words, ACQ1 3104 and ACQ2 3102 select a long time constant for DC offset acquisition. In an embodiment, WC reset signal 4308 is equal to 0. State 4608 is active as long as a receiving mode is maintained, and a diversity transition does not occur. If a diversity transition occurs while state 4612 is active (i.e., B[0] is not equal to b[0]), the active state transitions from state 4612 back to state 4608 via a transition 4630. When PCM is set to be equal to a setting other than 11, the active state transitions from state 4612 to state 4604, via a transition 4632.

[0341] FIG. 47 shows a state diagram 4700, according to an exemplary alternative embodiment of the present invention. State diagram 4700 may be implemented in state machine module 4500 to generate signals ACQ1 3104, ACQ2 3102, and WC reset signal 4308. State diagram 4700 includes states 4702, 4704, 4706, 4708, 4710, 4712, 4734, 4736, and 4746. State diagram 4700 is similar to state diagram 4600 in using PCM and b[0]/B[0] as input signals, while additionally using WC signal 4106 (shown in FIG. 41) as an input signal. In state diagram 4700, when WC signal 4106 is received, changes to states of ACQ may occur, such that changes in the DC offset voltage acquisition time constant are made. For example, a change in WC signal 4106 may cause a change from a medium time constant to a long time constant, and vice versa. State diagram 4700 is particularly applicable to a WLAN environment, and is applicable to both short preamble (e.g., 56 μS) and long preamble (e.g., 128 μS) data frames, for example.

[0342] It should be understood that the above state machine and state diagram examples are provided for illustrative purposes only. The invention is not limited to these embodiments. Alternate embodiments (including equivalents, extensions, variations, deviations, etc., of the embodiments described herein) will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein. For

example, diversity signal 4505 may provide further bits of information that control the operation of state machine 4500. Diversity signal 4505 may instruct state machine 4500 to cause changes in the DC offset voltage acquisition time constant at each diversity antenna transition. For example, a change to a short time constant may be inserted at a diversity antenna transition, for a duration of 1 μS, 2 μS, or 4 μS, for instance. In another example, a setting for diversity signal 4505 may instruct state machine 4500 to use WC signal 4106 to control the DC offset voltage acquisition time constant, such that changes between short, medium, and long time constants may occur as necessary. These changes may be implemented by the addition/modification of states in state diagrams 4600 and/or 4700. The invention is intended and adapted to include such alternate embodiments.

5. Conclusion

[0343] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. It will be apparent to persons skilled in the relevant art that various changes in form and detail can be made therein without departing from the spirit and scope of the invention. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.